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23	COM, F_USB, R_USB, I_PWR
24	ALC887R CODEC
25	AUDIO JACK

[illegible]

Model Name:GA-970A-DS3

Component value change history


Version: 3.0

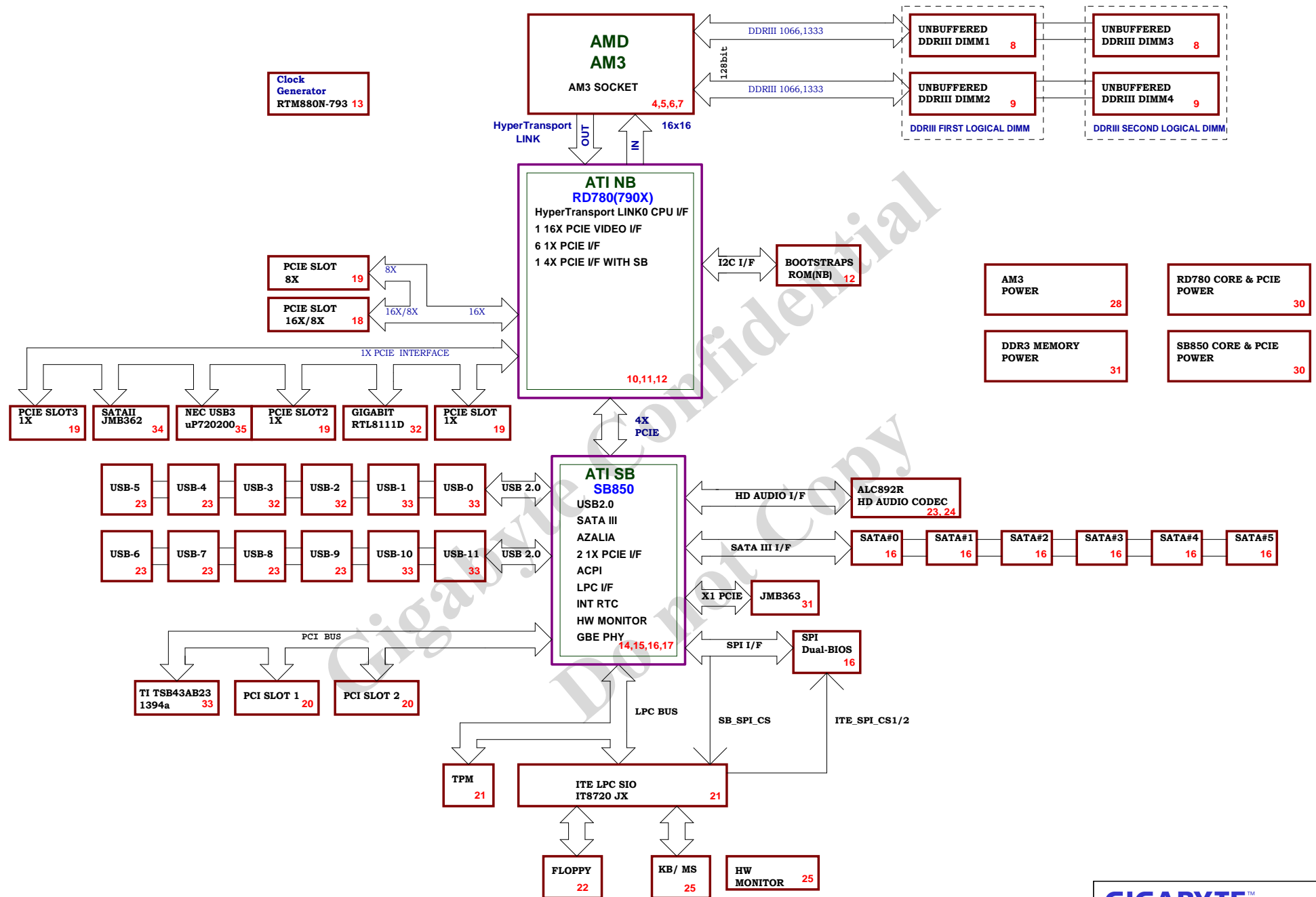
P-Code: U98094-0

[illegible]

Circuit or PCB layout change for next version

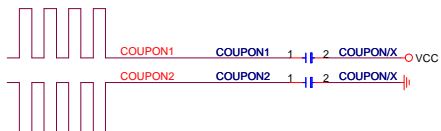
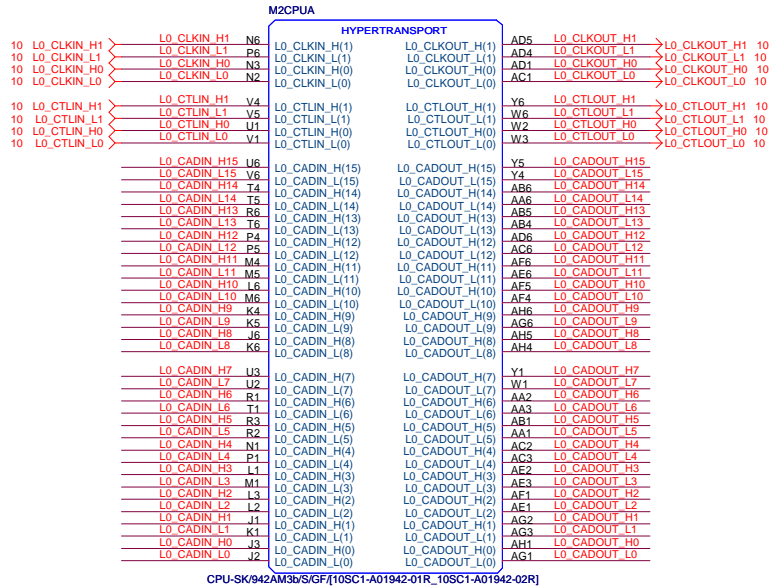
[illegible]

			
Title			
BOM & PCB HISTORY			
Size	Document Number	Rev	
Custom	GA-970A-DS3	3.0	
Date:	Tuesday, September 25, 2012	Sheet	2 of 36

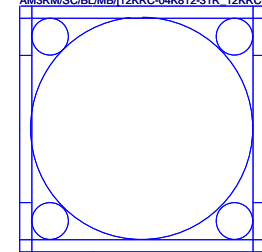


CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

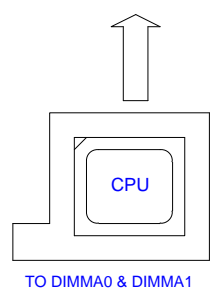
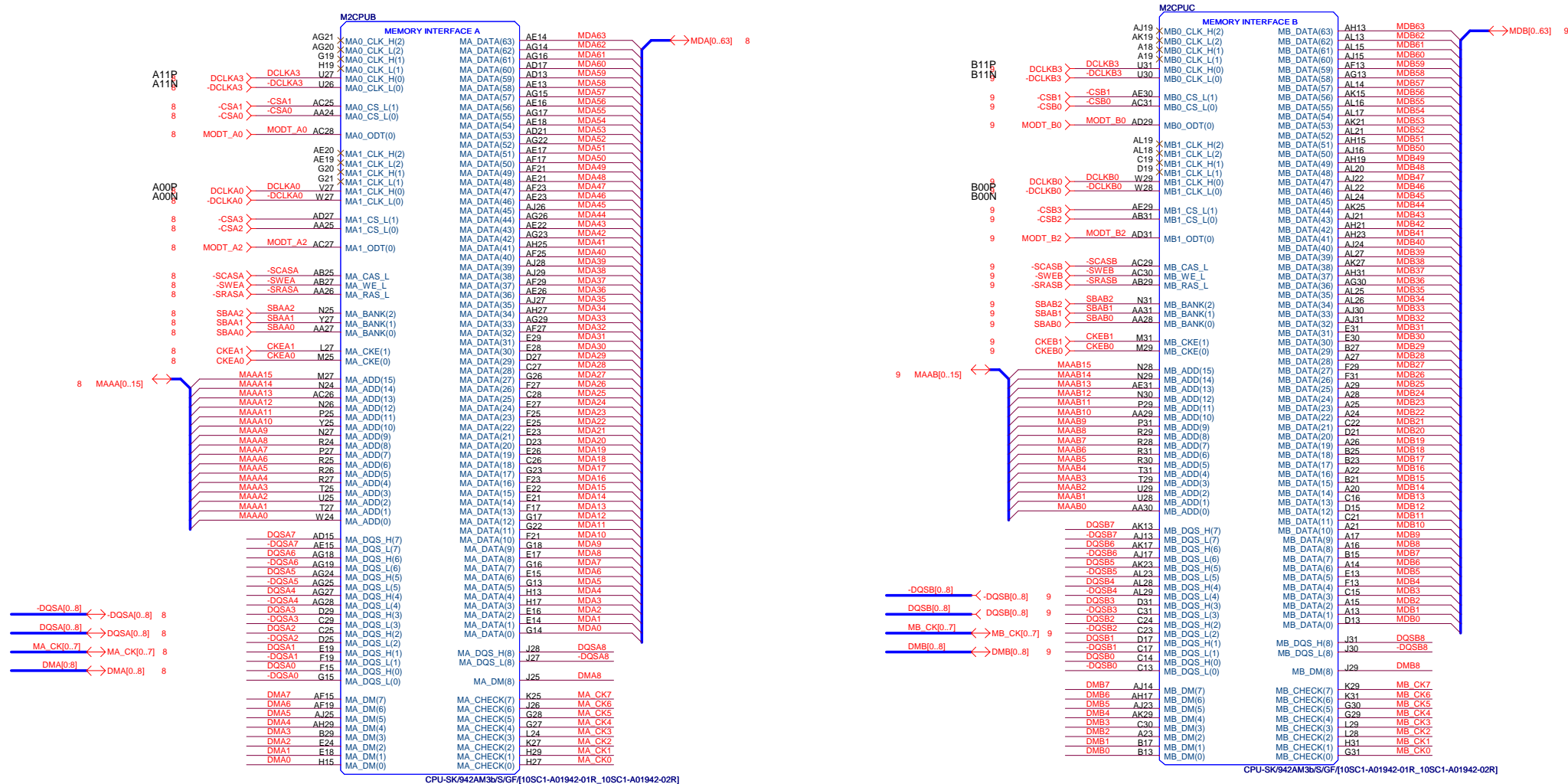
VLDT_A = VCC12_HT
 VLDT_B = HT12B



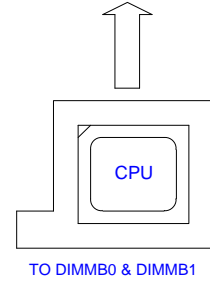
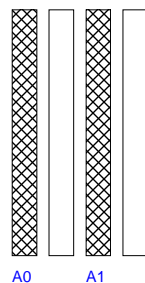
M2CPU
 AM3RM/SC/BL/MB/12KRC-04K812-31R_12KRC-04K812-32R]



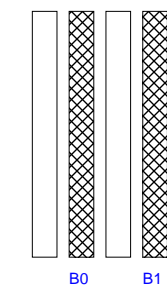
GIGABYTE™			
Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custom	GA-970A-DS3	3.0	
Date:	Friday, September 21, 2012	Sheet	4 of 36

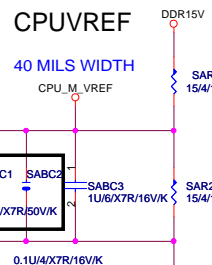
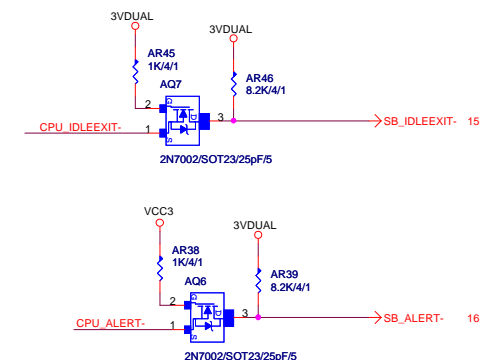
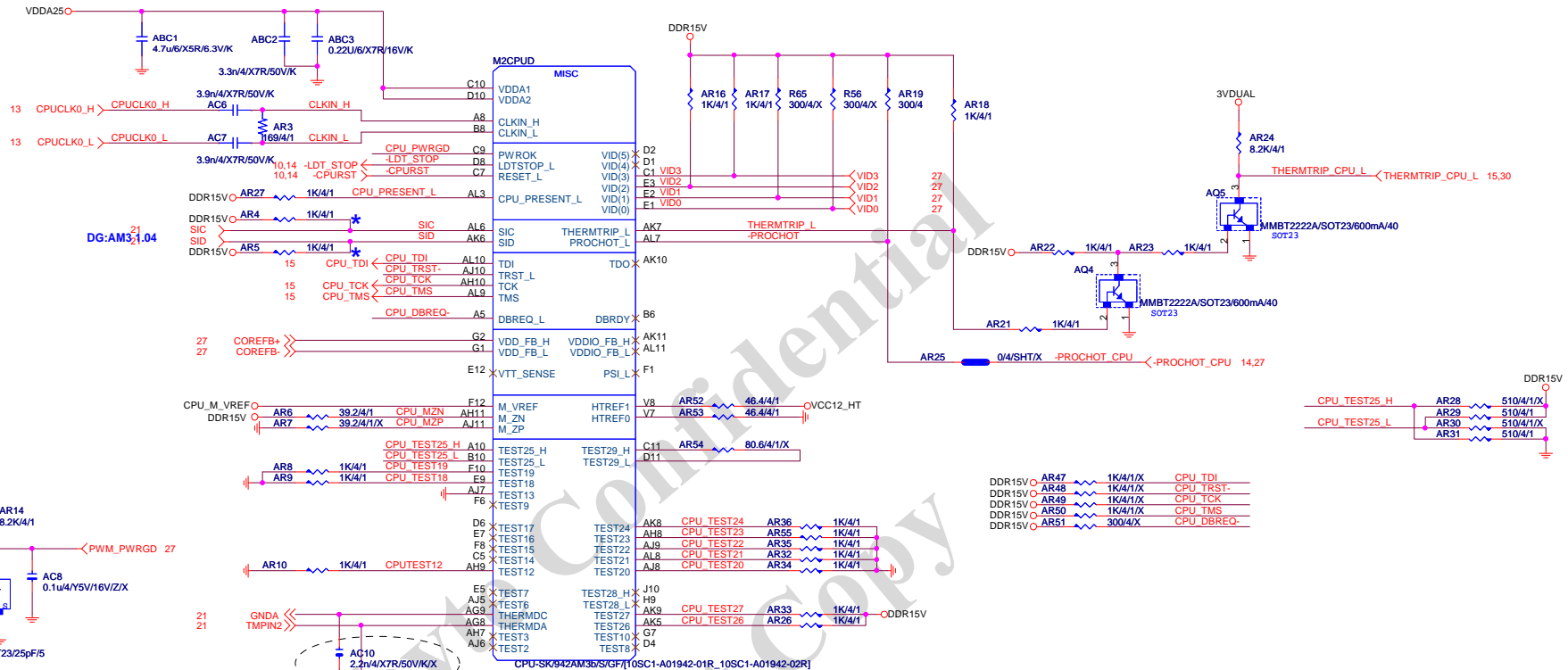


MEM CHA

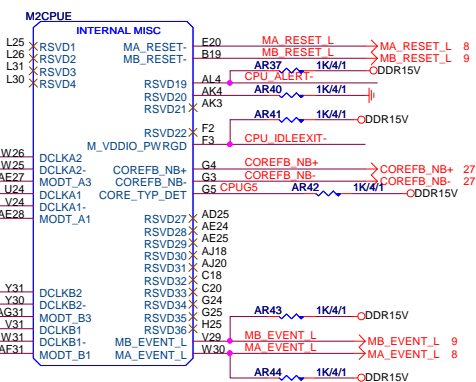


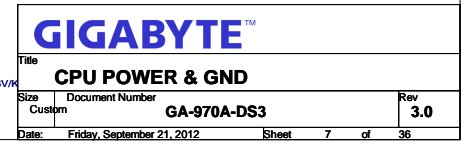
MEM CHB

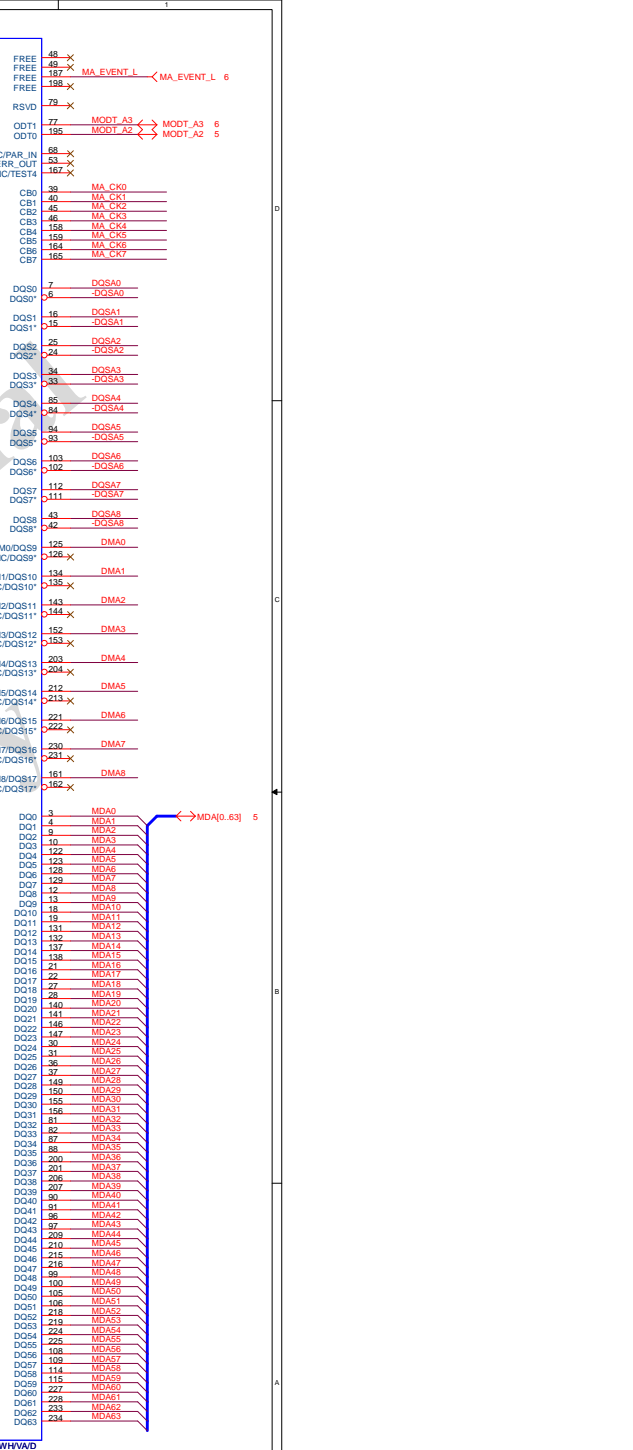
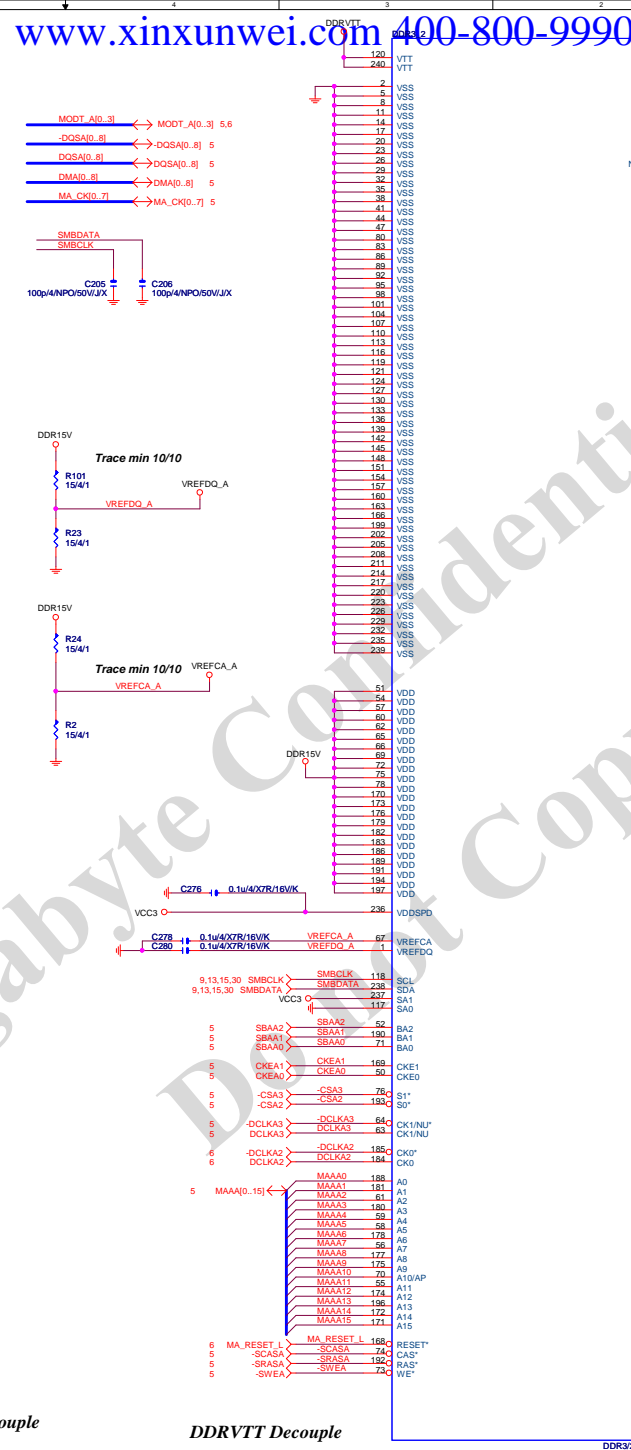
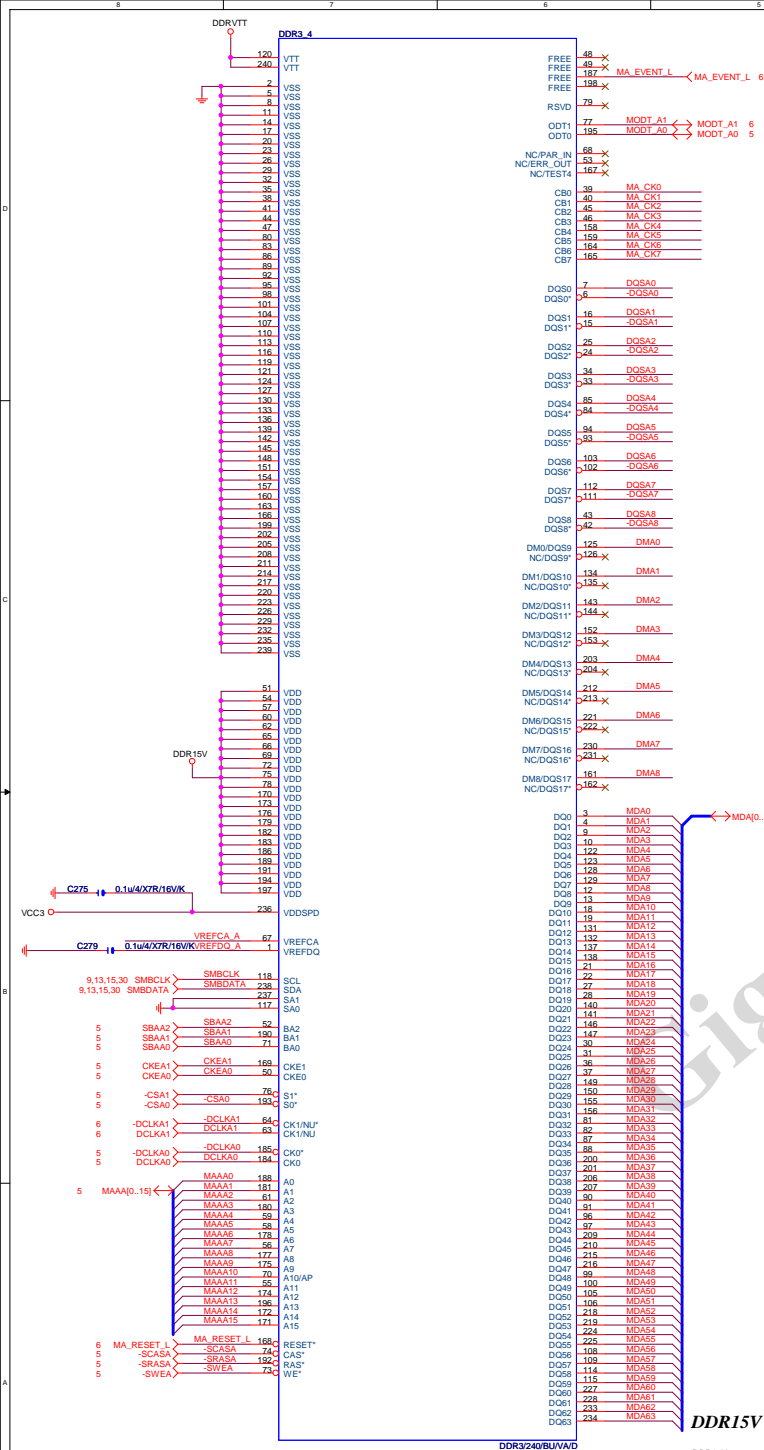


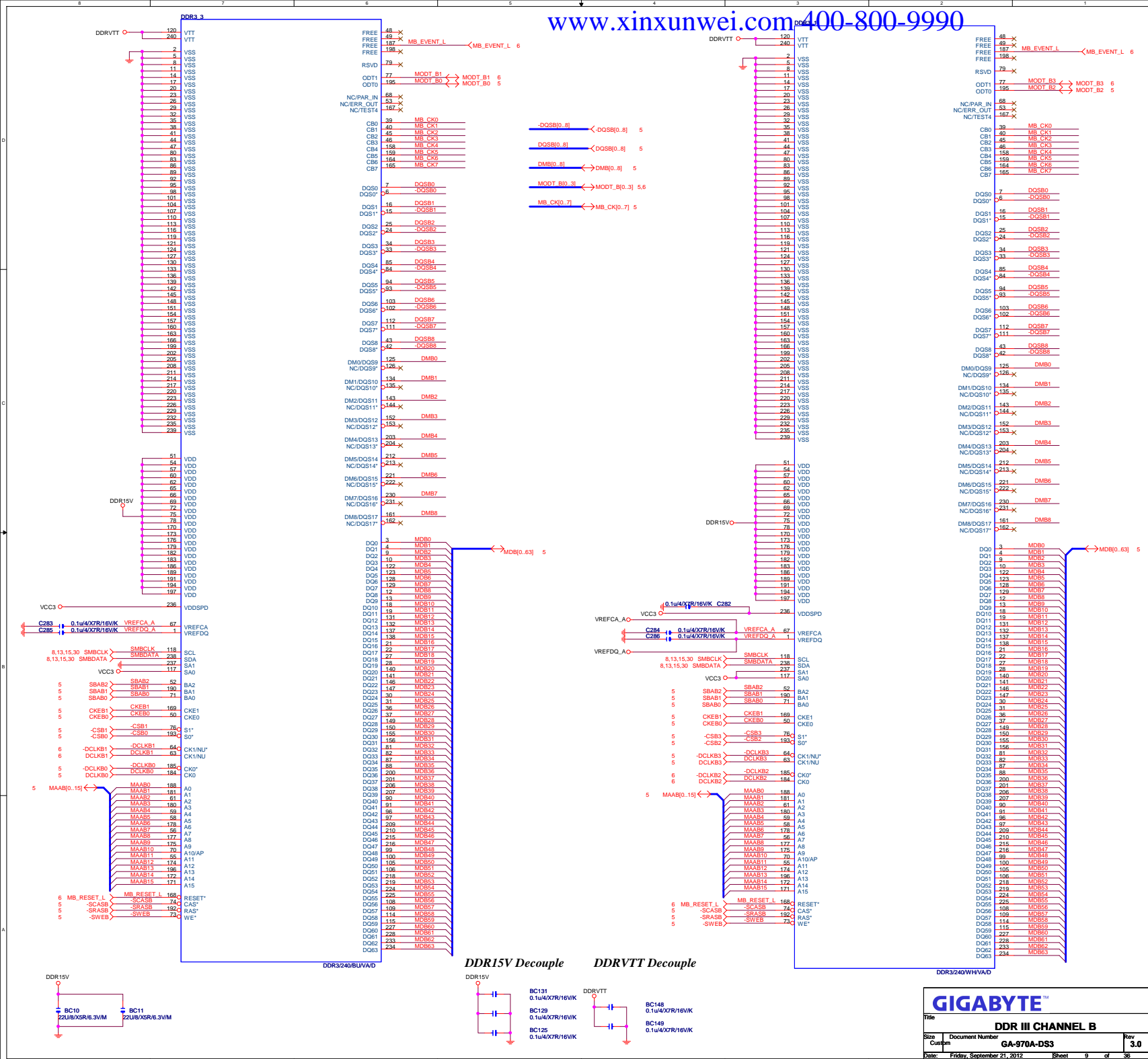


Layout: Place within 500mils of the CPU socket.







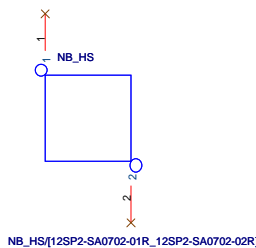
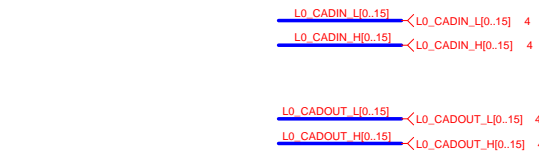
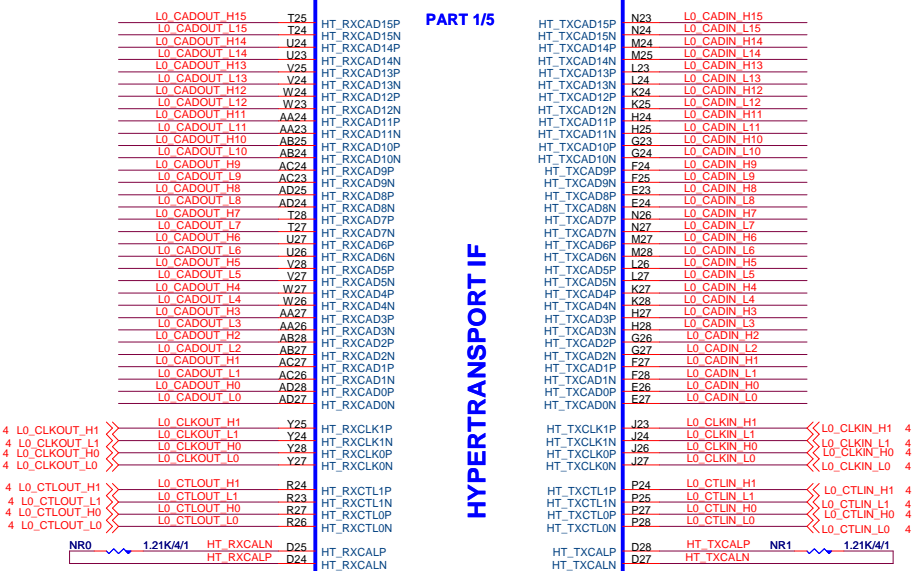


U3A

PART 1/5

HYPERTRANSPORT IF

RX980/BGA692



NB_HS[12SP2-SA0702-01R_12SP2-SA0702-02R]

U3C

PART 3/5
CLOCKS

PM

MISC.

STRP_DATA

TESTMODE

DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEB

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101 : 2:2:2:4 C2
110 : Hardware default (mode L) or EEPROM
111 : Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEB

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

GIGABYTE™

Title RS780 HT-LINK V/F

Size Custom Document Number GA-970A-DS3 Rev 3.0
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U3B

PART 2/5

EXP A_RXP15 N6
EXP A_RXN15 N5
EXP A_RXP14 M5
EXP A_RXN14 M4
EXP A_RXP13 L6
EXP A_RXN13 L5
EXP A_RXP12 K5
EXP A_RXN12 K4
EXP A_RXP11 J6
EXP A_RXN11 J5
EXP A_RXP10 H5
EXP A_RXN10 H4
EXP A_RXP9 G6
EXP A_RXN9 G5
EXP A_RXP8 F5
EXP A_RXN8 F4
EXP A_RXP7 D2
EXP A_RXN7 D1
EXP A_RXP6 B5
EXP A_RXN6 B4
EXP A_RXP5 C6
EXP A_RXN5 E6
EXP A_RXP4 E7
EXP A_RXN4 F7
EXP A_RXP3 D8
EXP A_RXN3 E8
EXP A_RXP2 E9
EXP A_RXN2 F9
EXP A_RXP1 D10
EXP A_RXN1 E10
EXP A_RXP0 E11
EXP A_RXN0 F11

GPP1_RX15P
GPP1_RX15N
GPP1_RX14P
GPP1_RX14N
GPP1_RX13P
GPP1_RX13N
GPP1_RX12P
GPP1_RX12N
GPP1_RX11P
GPP1_RX11N
GPP1_RX10P
GPP1_RX10N
GPP1_RX9P
GPP1_RX9N
GPP1_RX8P
GPP1_RX8N
GPP1_RX7P
GPP1_RX7N
GPP1_RX6P
GPP1_RX6N
GPP1_RX5P
GPP1_RX5N
GPP1_RX4P
GPP1_RX4N
GPP1_RX3P
GPP1_RX3N
GPP1_RX2P
GPP1_RX2N
GPP1_RX1P
GPP1_RX1N
GPP1_RX0P
GPP1_RX0N

PCIE GPP1

GPP2_TX15P
GPP2_TX15N
GPP2_TX14P
GPP2_TX14N
GPP2_TX13P
GPP2_TX13N
GPP2_TX12P
GPP2_TX12N
GPP2_TX11P
GPP2_TX11N
GPP2_TX10P
GPP2_TX10N
GPP2_TX9P
GPP2_TX9N
GPP2_TX8P
GPP2_TX8N
GPP2_TX7P
GPP2_TX7N
GPP2_TX6P
GPP2_TX6N
GPP2_TX5P
GPP2_TX5N
GPP2_TX4P
GPP2_TX4N
GPP2_TX3P
GPP2_TX3N
GPP2_TX2P
GPP2_TX2N
GPP2_TX1P
GPP2_TX1N
GPP2_TX0P
GPP2_TX0N

N3
M2
M1
L3
L2
K2
K1
J3
J2
H2
H1
G3
G2
F2
F1
E3
E2
A4
A3
A2
A1
B6
B5
B4
B3
B2
B1
C11

EXP A_TXP15
EXP A_TXN15
EXP A_TXP14
EXP A_TXN14
EXP A_TXP13
EXP A_TXN13
EXP A_TXP12
EXP A_TXN12
EXP A_TXP11
EXP A_TXN11
EXP A_TXP10
EXP A_TXN10
EXP A_TXP9
EXP A_TXN9
EXP A_TXP8
EXP A_TXN8
EXP A_TXP7
EXP A_TXN7
EXP A_TXP6
EXP A_TXN6
EXP A_TXP5
EXP A_TXN5
EXP A_TXP4
EXP A_TXN4
EXP A_TXP3
EXP A_TXN3
EXP A_TXP2
EXP A_TXN2
EXP A_TXP1
EXP A_TXN1
EXP A_TXP0
EXP A_TXN0

AC9
AD9
AE8
AE7
AD7
AD6
AE6
AE5
AG5
AF2
AD2
AD1
AB5
AB4
AA6
AA5
Y5
Y4
W6
W5
V5
V4
U6
U5
T5
T4
R6
R5
P5
P4

GPP2_RX15P
GPP2_RX15N
GPP2_RX14P
GPP2_RX14N
GPP2_RX13P
GPP2_RX13N
GPP2_RX12P
GPP2_RX12N
GPP2_RX11P
GPP2_RX11N
GPP2_RX10P
GPP2_RX10N
GPP2_RX9P
GPP2_RX9N
GPP2_RX8P
GPP2_RX8N
GPP2_RX7P
GPP2_RX7N
GPP2_RX6P
GPP2_RX6N
GPP2_RX5P
GPP2_RX5N
GPP2_RX4P
GPP2_RX4N
GPP2_RX3P
GPP2_RX3N
GPP2_RX2P
GPP2_RX2N
GPP2_RX1P
GPP2_RX1N
GPP2_RX0P
GPP2_RX0N

PCIE GPP2

GPP3_RX9P
GPP3_RX9N
GPP3_RX8P
GPP3_RX8N
GPP3_RX7P
GPP3_RX7N
GPP3_RX6P
GPP3_RX6N
GPP3_RX5P
GPP3_RX5N
GPP3_RX4P
GPP3_RX4N
GPP3_RX3P
GPP3_RX3N
GPP3_RX2P
GPP3_RX2N
GPP3_RX1P
GPP3_RX1N
GPP3_RX0P
GPP3_RX0N

AF9
AG9
AG8
AH8
AF7
AG7
AG6
AH6
AG4
AH4
AE3
AE2
AC3
AC2
AB2
AB1
AA3
AA2
Y2
Y1
W3
W2
V2
V1
U3
U2
T2
T1
R3
R2
P2
P1

AD11
AC11
AE12
AD12
AD13
AC13
AE14
AD14
AD15
AC15
AE16
AD16
AD17
AC17
AE18
AD18
AD19
AC19
AH20
AG20

GPP3_RX9P
GPP3_RX9N
GPP3_RX8P
GPP3_RX8N
GPP3_RX7P
GPP3_RX7N
GPP3_RX6P
GPP3_RX6N
GPP3_RX5P
GPP3_RX5N
GPP3_RX4P
GPP3_RX4N
GPP3_RX3P
GPP3_RX3N
GPP3_RX2P
GPP3_RX2N
GPP3_RX1P
GPP3_RX1N
GPP3_RX0P
GPP3_RX0N

PCIE GPP3

GPP3_TX9P
GPP3_TX9N
GPP3_TX8P
GPP3_TX8N
GPP3_TX7P
GPP3_TX7N
GPP3_TX6P
GPP3_TX6N
GPP3_TX5P
GPP3_TX5N
GPP3_TX4P
GPP3_TX4N
GPP3_TX3P
GPP3_TX3N
GPP3_TX2P
GPP3_TX2N
GPP3_TX1P
GPP3_TX1N
GPP3_TX0P
GPP3_TX0N

AH10
AG10
AG11
AE15
AH12
AG12
AG13
AE13
AH14
AG14
AG15
AG16
AH18
AG18
AG17
AH17
AG19
AH19

PCI_E slot TX need CAP close to slot side

EXP A_TXP[0..15] >> EXP_A_TXP[0..15] 18

EXP A_TXN[0..15] >> EXP_A_TXN[0..15] 18

EXP A_RXP[0..15] >> EXP_A_RXP[0..15] 18

EXP A_RXN[0..15] >> EXP_A_RXN[0..15] 18

19 PCIE5_IP
19 PCIE5_IN
33 ML_IP
33 ML_IN

PCIE5_IP
PCIE5_IN
ML_IP
ML_IN

AC15
AE16
AD16
AD17
AC17
AE18
AD18
AD19
AC19
AH20
AG20

GPP3_RX5P
GPP3_RX5N
GPP3_RX4P
GPP3_RX4N
GPP3_RX3P
GPP3_RX3N
GPP3_RX2P
GPP3_RX2N
GPP3_RX1P
GPP3_RX1N
GPP3_RX0P
GPP3_RX0N

GPP3_TX5P
GPP3_TX5N
GPP3_TX4P
GPP3_TX4N
GPP3_TX3P
GPP3_TX3N
GPP3_TX2P
GPP3_TX2N
GPP3_TX1P
GPP3_TX1N
GPP3_TX0P
GPP3_TX0N

NC4
NC3
NC6
NC5

0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK

PCIE5_OP
PCIE5_ON
ML_OP
ML_ON

19
19
33
33

19 PCIE2_IP
19 PCIE2_IN
19 PCIE1_IP
19 PCIE1_IN
31 USB3_IP
31 USB3_IN

PCIE2_IP
PCIE2_IN
PCIE1_IP
PCIE1_IN
USB3_IP
USB3_IN

AD18
AD19
AC19
AH20
AG20

GPP3_RX2P
GPP3_RX2N
GPP3_RX1P
GPP3_RX1N
GPP3_RX0P
GPP3_RX0N

GPP3_TX2P
GPP3_TX2N
GPP3_TX1P
GPP3_TX1N
GPP3_TX0P
GPP3_TX0N

NC10
NC9
NC20
NC19
NC2
NC1

0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK

PCIE2_OP
PCIE2_ON
PCIE1_OP
PCIE1_ON
USB3_OP
USB3_ON

19
19
18
19
31
31

14 A_RX3P
14 A_RX3N
14 A_RX2P
14 A_RX2N
14 A_RX1P
14 A_RX1N
14 A_RX0P
14 A_RX0N

AC21
AD21
AE22
AF25
AG25
AG26
AH26

SB_RX3P
SB_RX3N
SB_RX2P
SB_RX2N
SB_RX1P
SB_RX1N
SB_RX0P
SB_RX0N

PCIE ALINK

SB_TX3P
SB_TX3N
SB_TX2P
SB_TX2N
SB_TX1P
SB_TX1N
SB_TX0P
SB_TX0N

AG22
AH22
AF21
AG21
AF23
AG23
AG24
AH24

A_TX3P C
A_TX3N C
A_TX2P C
A_TX2N C
A_TX1P C
A_TX1N C
A_TX0P C
A_TX0N C

NC11
NC12
NC14
NC13
NC15
NC16
NC18
NC17

0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK
0.1u/4X7R/16VK

A_TX3P
A_TX3N
A_TX2P
A_TX2N
A_TX1P
A_TX1N
A_TX0P
A_TX0N

14
14
14
14
14
14
14
14

PLACE THESE CAP CLOSE TO NB.



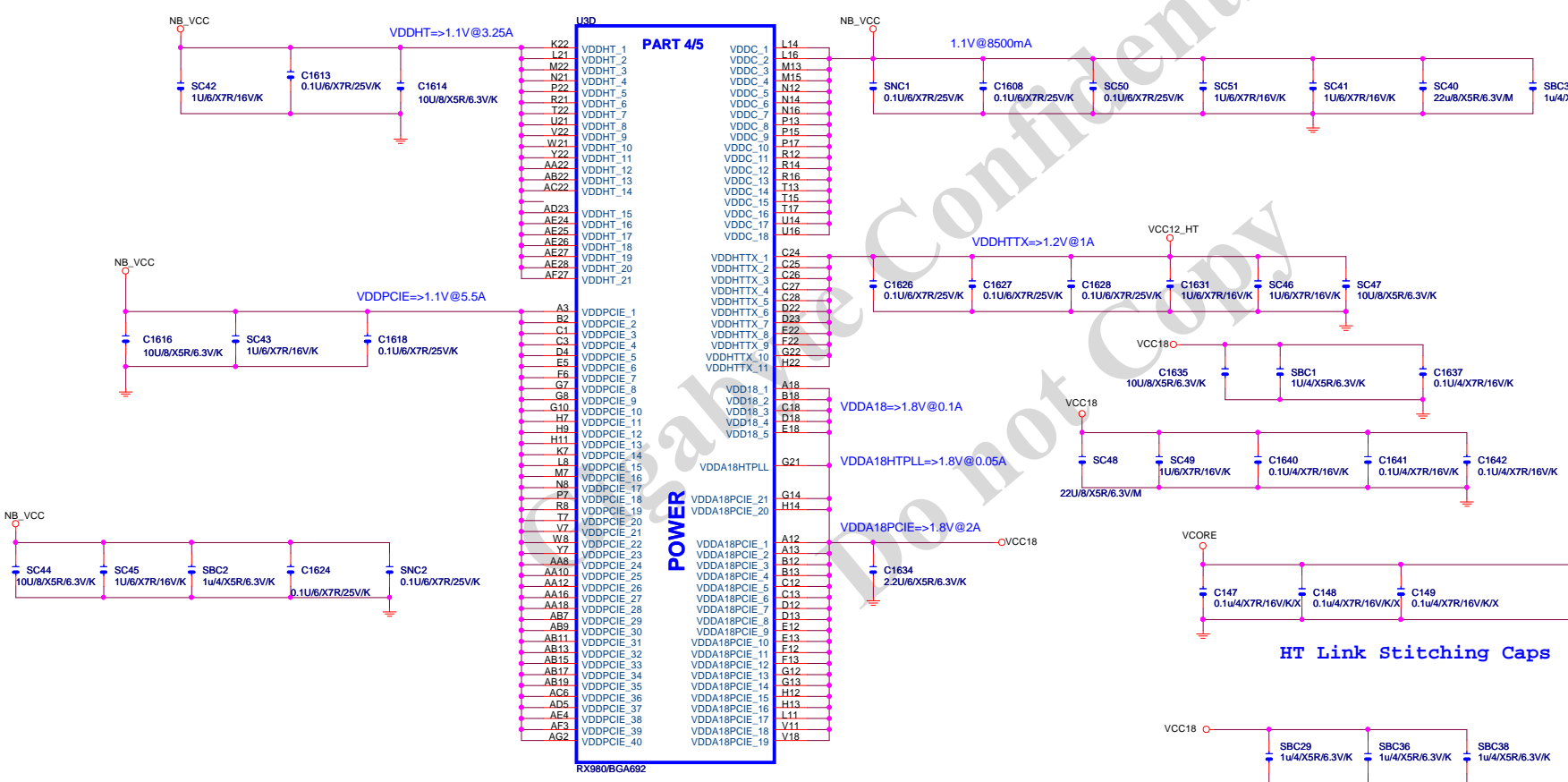
RX980/BGA692

GIGABYTE™

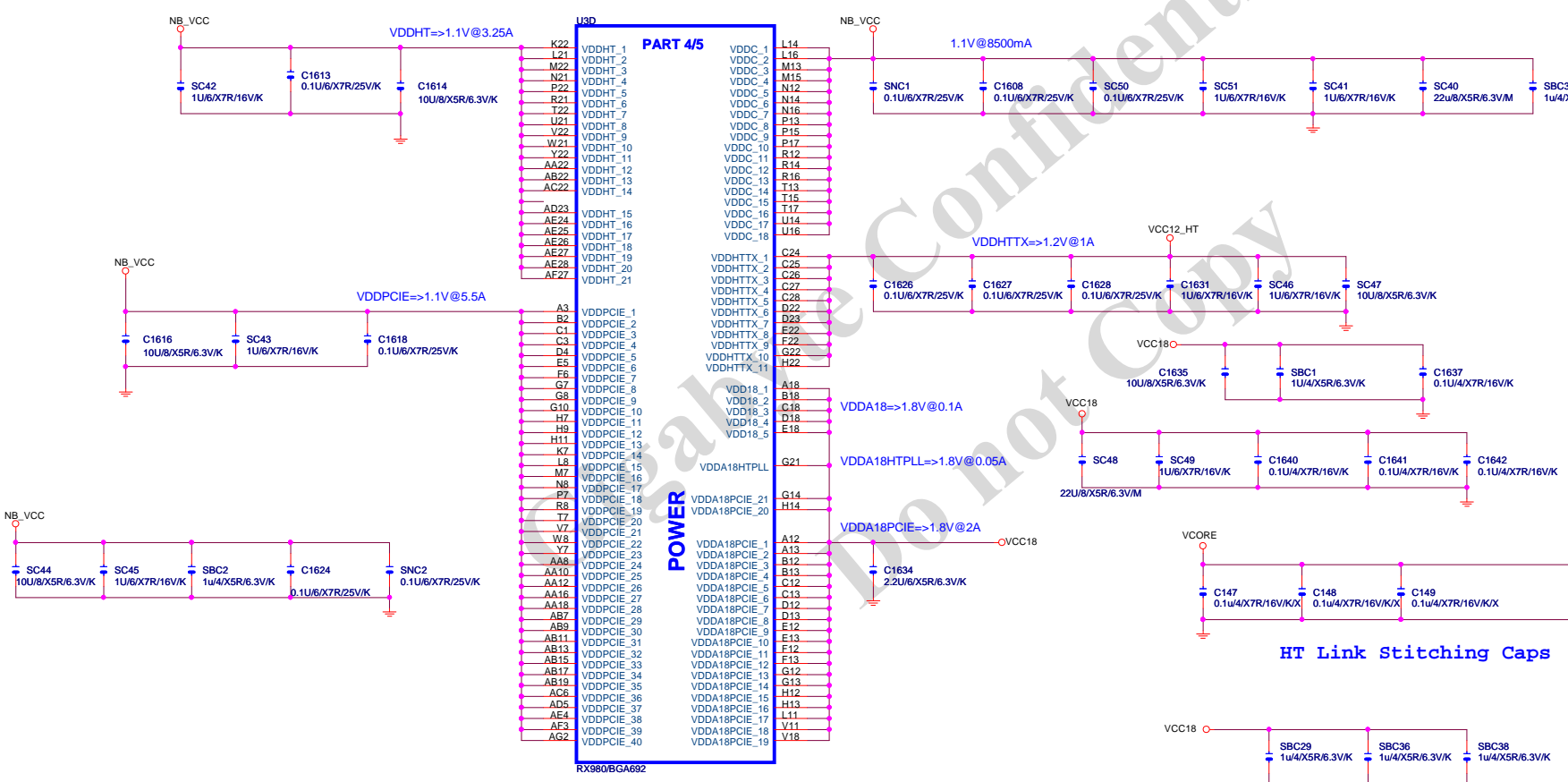
Title
RS780 PCIE I/F ,SwitchSize Document Number
Custom GA-970A-DS3Rev
3.0

Date: Friday, September 21, 2012 Sheet 11 of 36

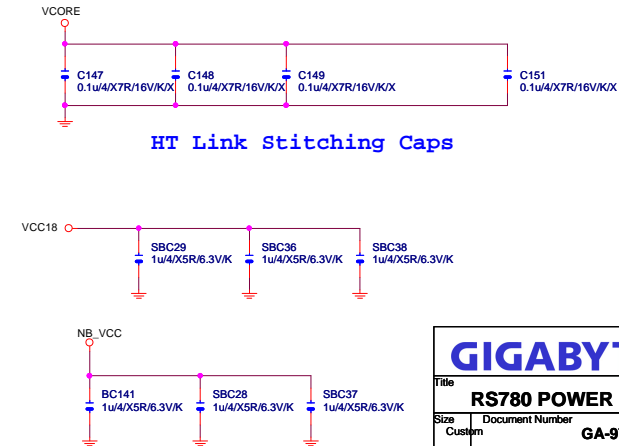
PART 4



POWER



HT Link Stitching Caps



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

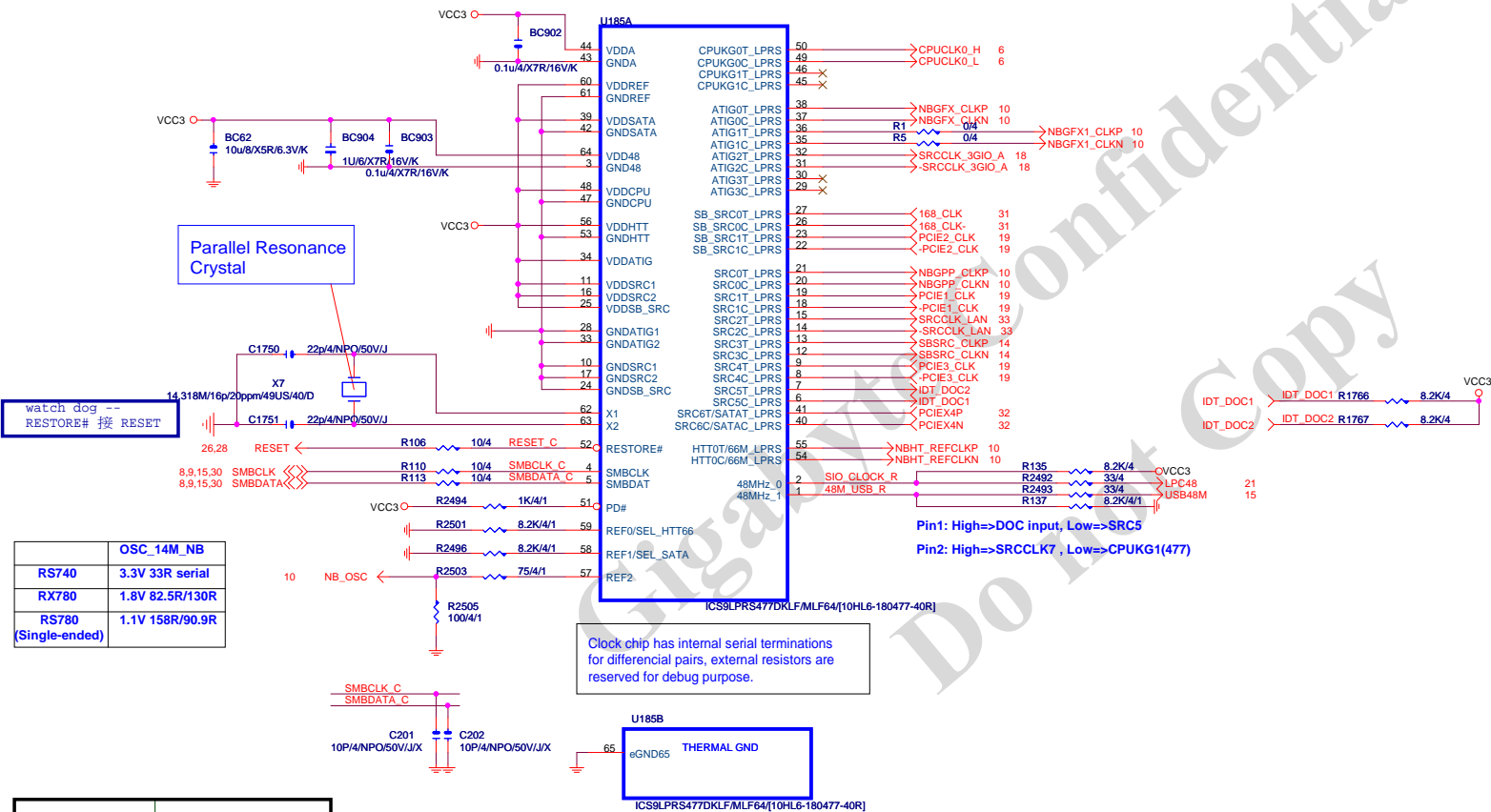
* the GFX_REFCLK input is required for all cases

1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

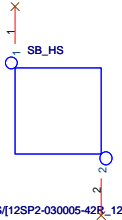
REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE™			
Title			
RTM880N-793			
Size	Document Number	Rev	
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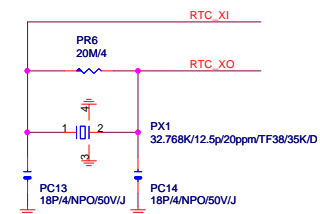


PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO SB850

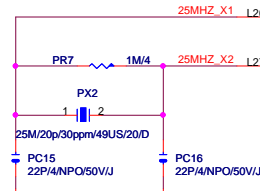
S.B HEATSINK

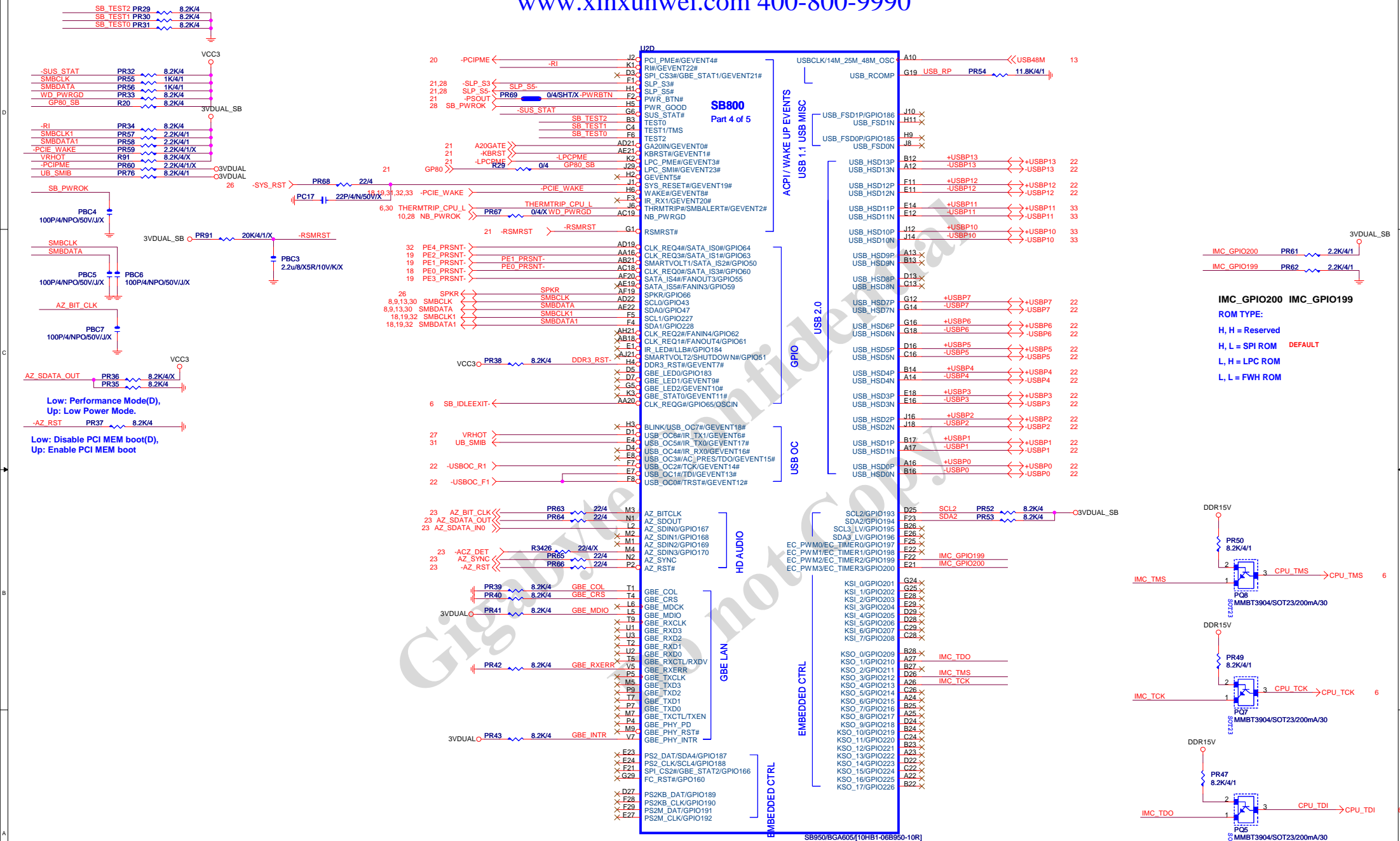


SB_HS[12SP2-030005-42B, 12SP2-030005-43R]



PX1
SHW/D0.64*5.08*6.74







PLACE SATA CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

VCC_SB0 PR75 1K/4/1 SATA_CALRP AB14
PR74 931/4/1 SATA_CALRN AA14

26 -SATA_LED -SATA_LED AD11

TP5 -SATA_X1 AD16

TP7 -SATA_X2 AC16

SB SPI DI PR70 22/4 SB SPI DI_R J5
SB SPI DO PR71 22/4 SB SPI DO_R F2
SB SPI CLK PR72 22/4 SB SPI CLK_R K4
SB SPI CS_ITE PR73 22/4 SB SPI CS_ K9
SB SPI CS_ITE PR73 22/4 SB SPI CS_ K9

SB950/BGA605(10HB1-06B950-10R)



PLACE SATA AC COUPLING
CAPS CLOSE TO SB850

SERIAL ATA

HW MONITOR

SPIROM

SB800
Part 2 of 5

GPIO

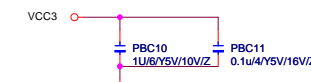
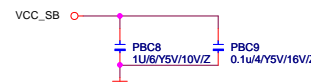
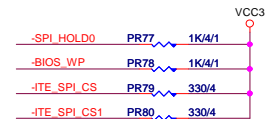
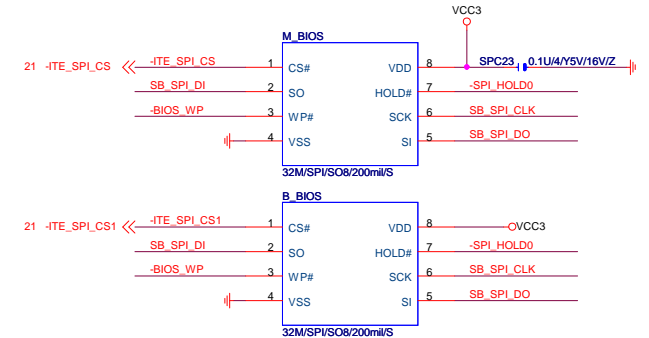
FC_CLK AH28
FC_FBCLKOUT AG28
FC_FBCLKIN AF28
FC_OE#/GPIO145 AF28
FC_AVDD#/GPIO146 AG28
FC_WVE#/GPIO148 AG28
FC_CE1#/GPIO149 AF28
FC_CE2#/GPIO150 AE28
FC_INT1/GPIO144 AF28
FC_INT2/GPIO147 AH28
FC_AD00/GPIO128 AJ27
FC_AD01/GPIO129 AJ26
FC_AD02/GPIO130 AH25
FC_AD03/GPIO131 AH24
FC_AD04/GPIO132 AG24
FC_AD05/GPIO133 AH23
FC_AD06/GPIO134 AJ23
FC_AD07/GPIO135 AJ22
FC_AD08/GPIO136 AF21
FC_AD08/GPIO137 AH22
FC_ADQ10/GPIO138 AJ22
FC_ADQ11/GPIO139 AJ24
FC_ADQ12/GPIO140 AJ25
FC_ADQ13/GPIO141 AJ25
FC_ADQ14/GPIO142 AG25
FC_ADQ15/GPIO143 AH25

FANOUT0/GPIO52 W5
FANOUT1/GPIO53 Y9
FANOUT2/GPIO54 Y9
FANIN0/GPIO56 W7
FANIN1/GPIO57 Y9
FANIN2/GPIO58 W8

TEMPIN0/GPIO171 B6
TEMPIN1/GPIO172 A6
TEMPIN2/GPIO173 A5
TEMPIN3/TALERT#/GPIO174 B5
TEMP_COMM C7

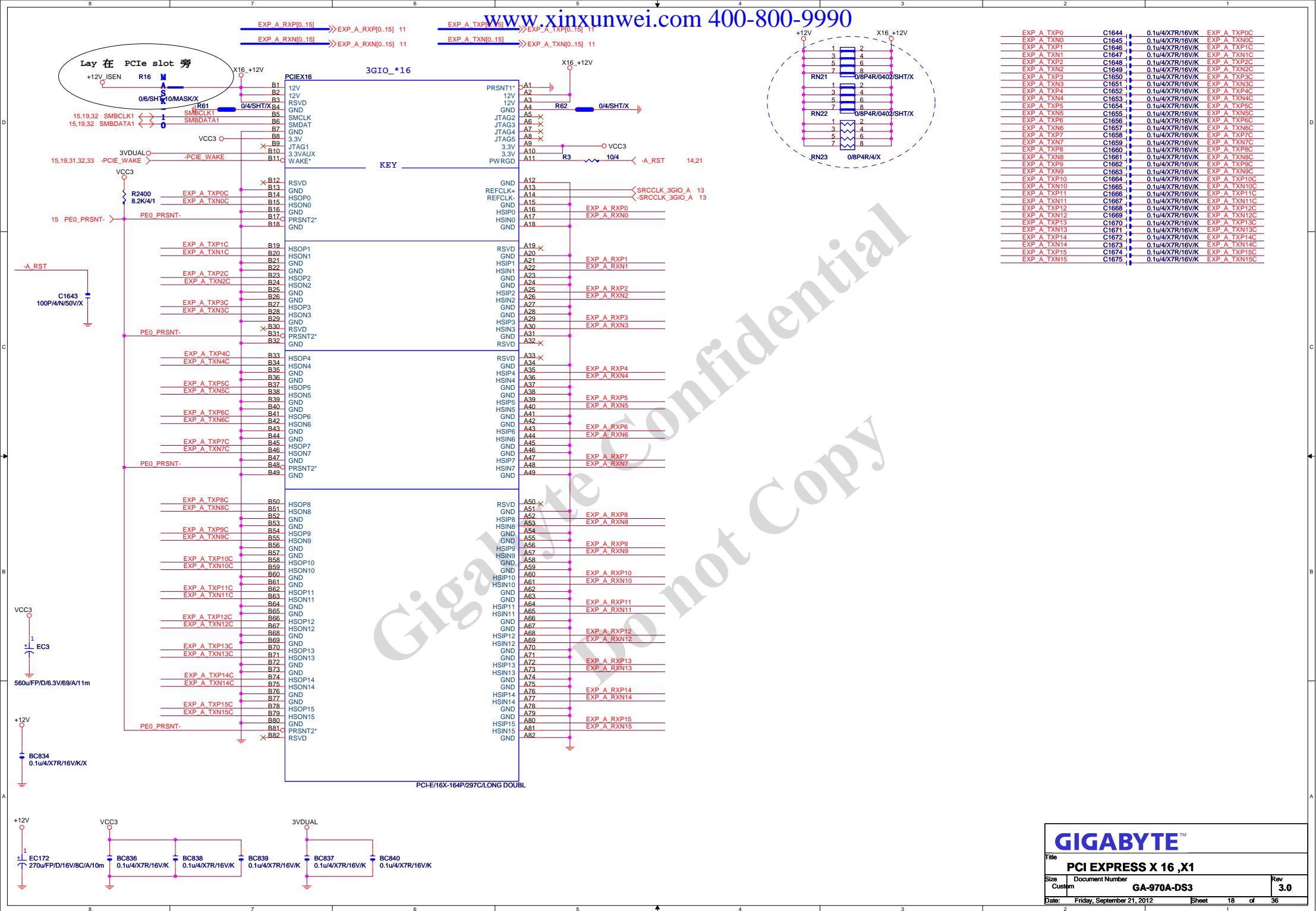
VIN0/GPIO175 A3
VIN1/GPIO176 B4
VIN2/GPIO177 B4
VIN3/GPIO178 C5
VIN4/GPIO179 A7
VIN5/GPIO180 B7
VIN6/GBE_STAT3/GPIO181 B8
VIN7/GBE_LED3/GPIO182 A8

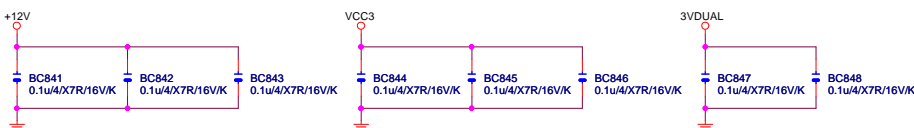
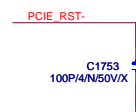
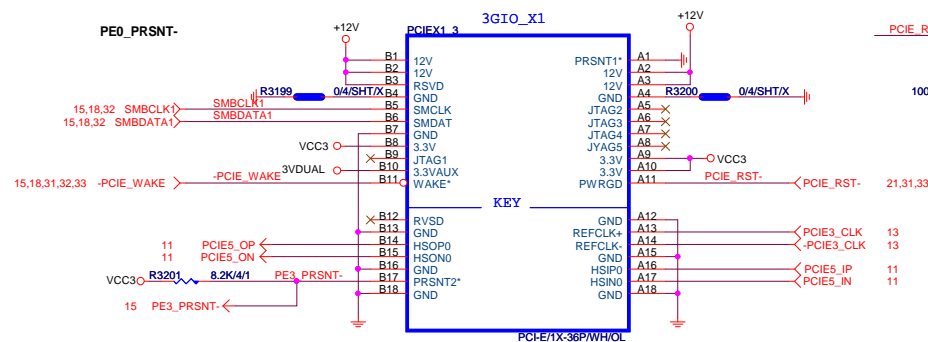
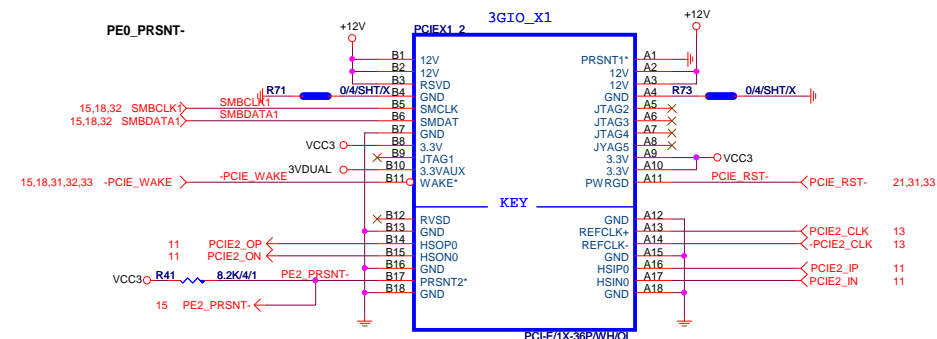
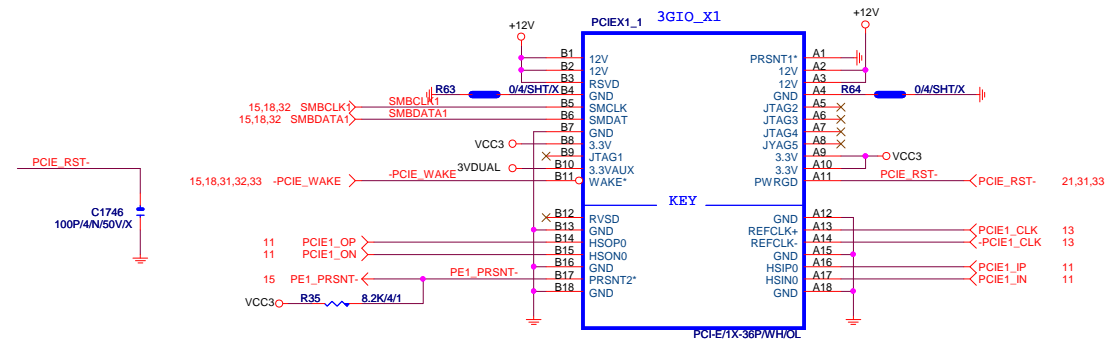
SPI DI/GPIO164 NC1 G27
SPI DO/GPIO163 NC2 Y2
SPI CLK/GPIO162 NC2 Y2
SPI CS#/GPIO165 NC2 Y2
ROM_RST#/GPIO161 NC2 Y2

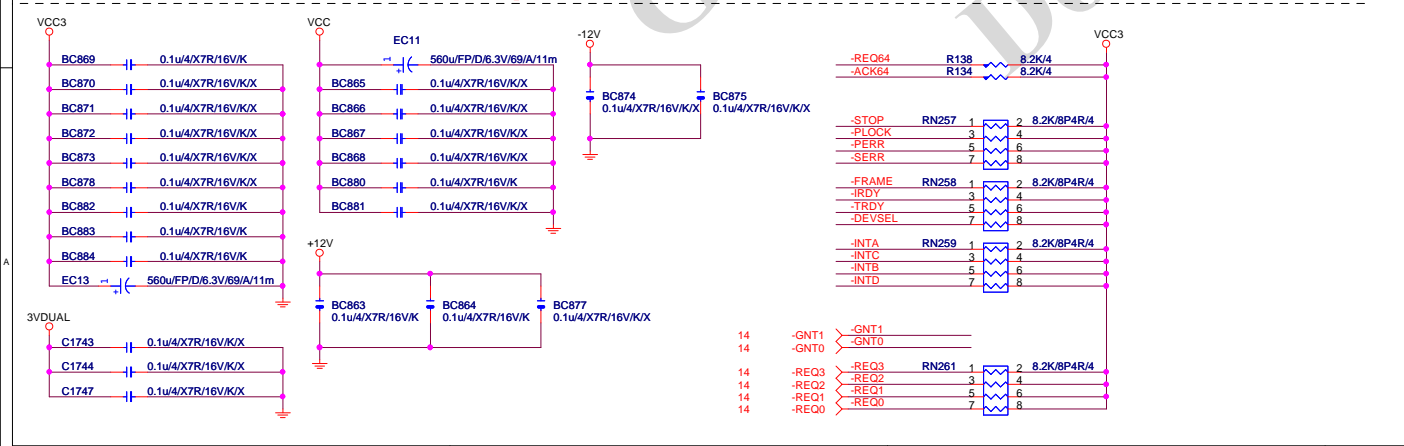


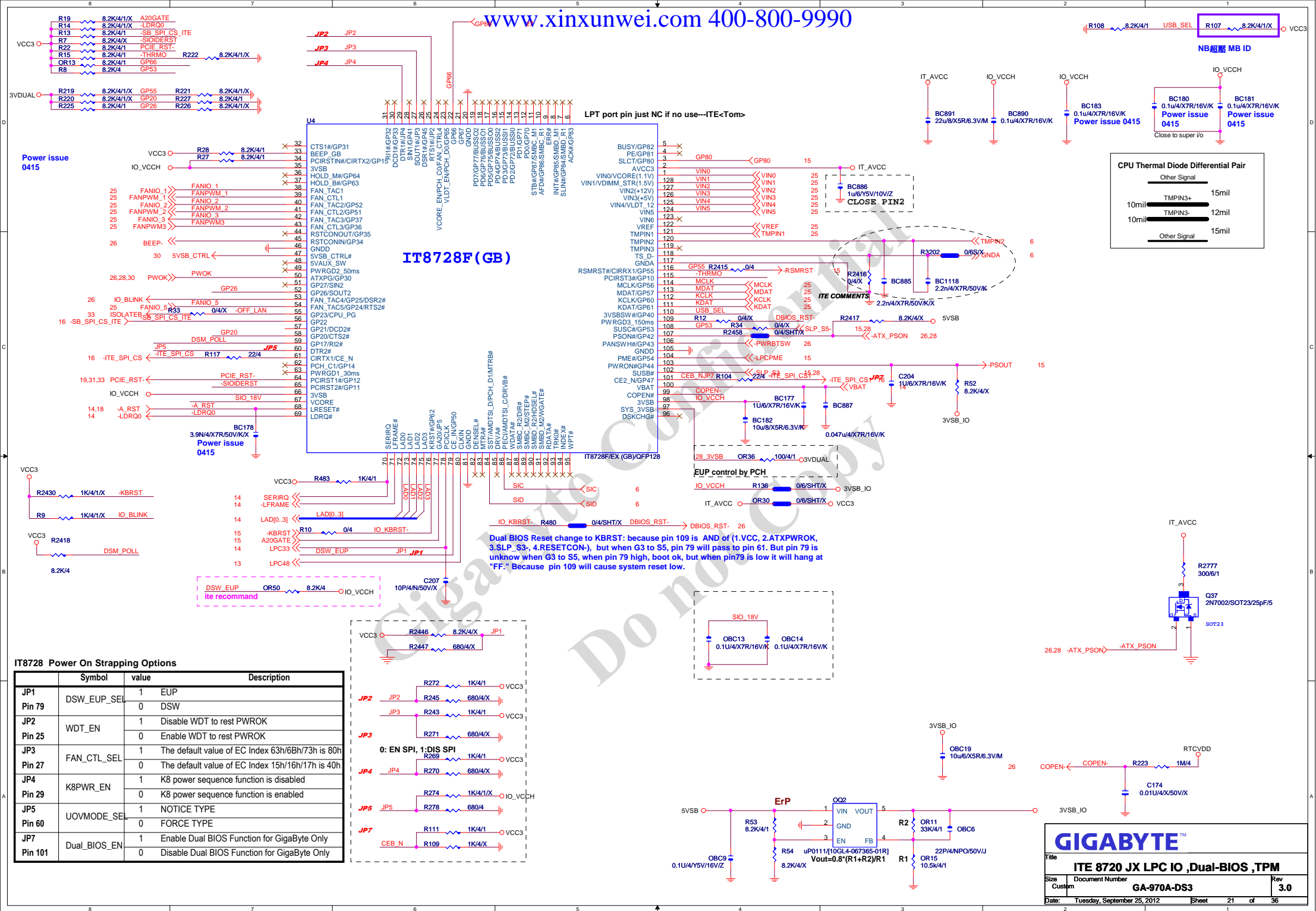
GIGABYTE ™		
Title ATI SB700 SATA/IDE/HWM/SPI		
Size	Document Number	Rev
Custom	GA-970A-DS3	3.0
Date:	Friday, September 21, 2012	Sheet 16 of 36

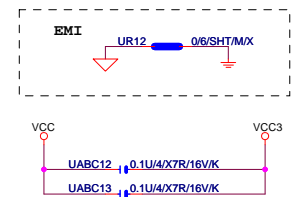
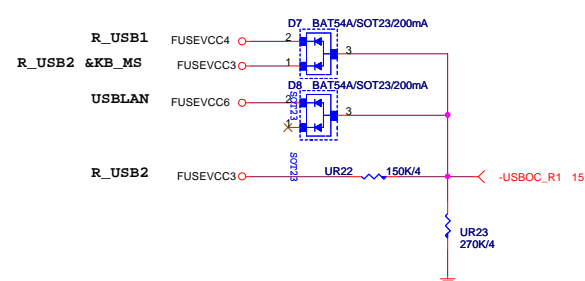
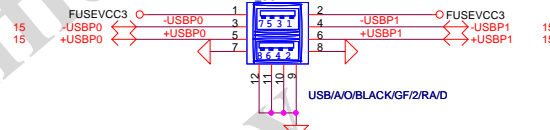
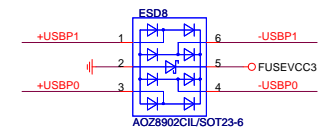
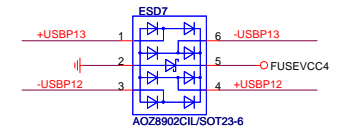
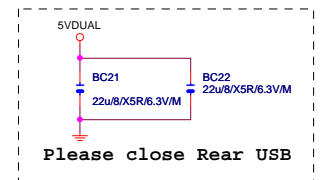
Title			
ATI SB700 POWER & GND			
Size	Document Number		Rev
Custom	GA-970A-DS3		3.0
Date:	Friday, September 21, 2012	Sheet	17 of 36











892WOR

For 892 with LDO

CR51
0/6

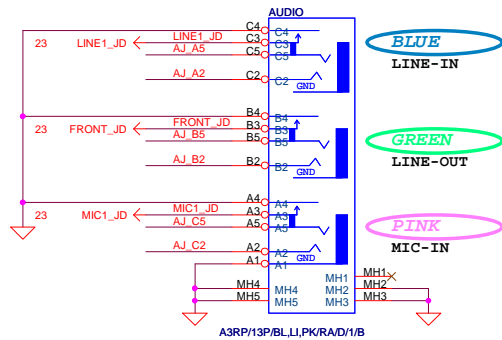
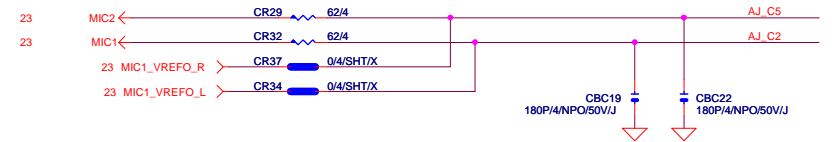
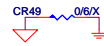
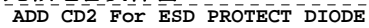
5VDUAL

CBC7
22u/8V5R/6.3V/M

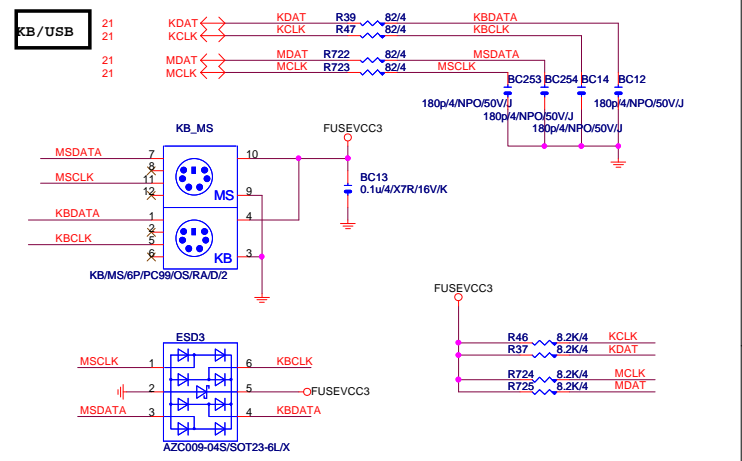
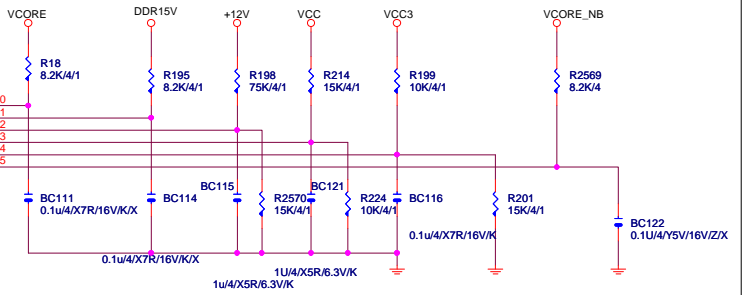
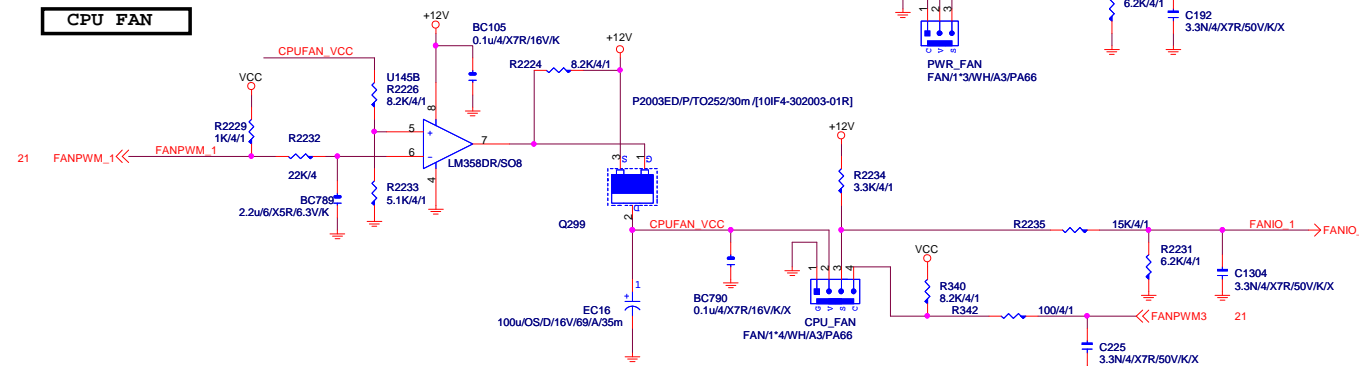
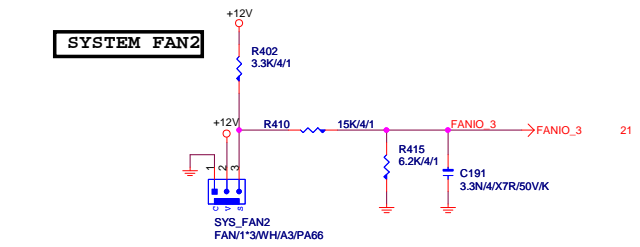
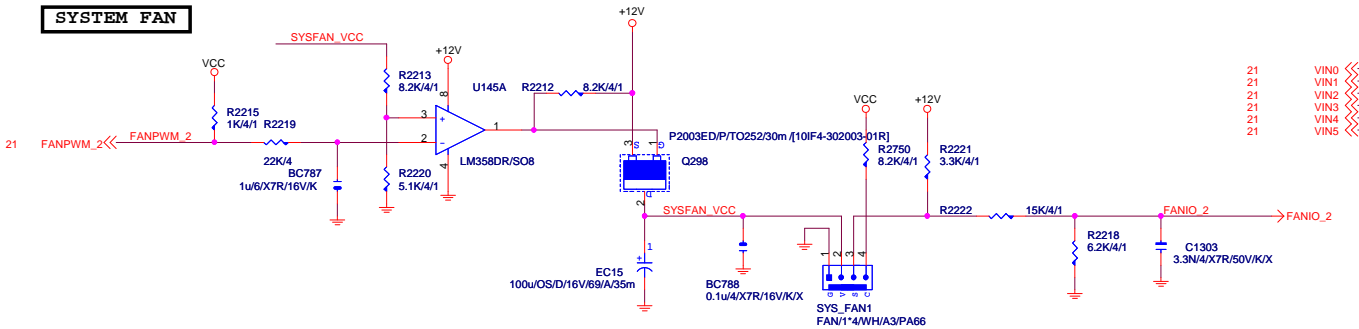
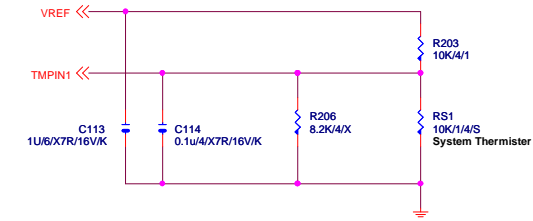
CD1

AZ2225-01L/SOD323

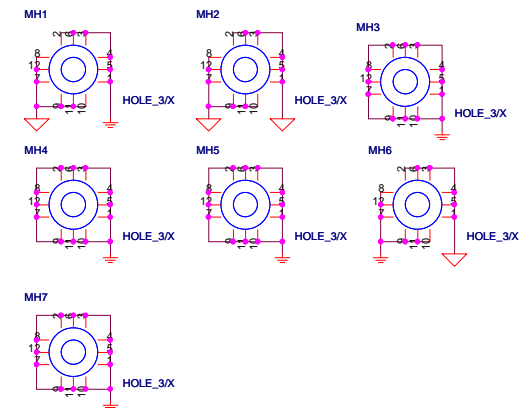
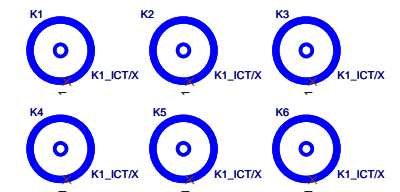
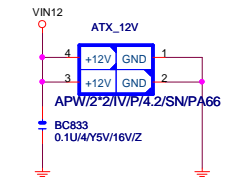
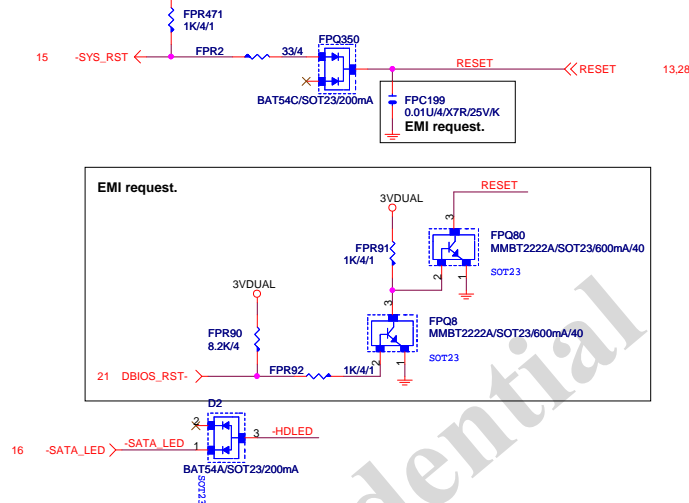
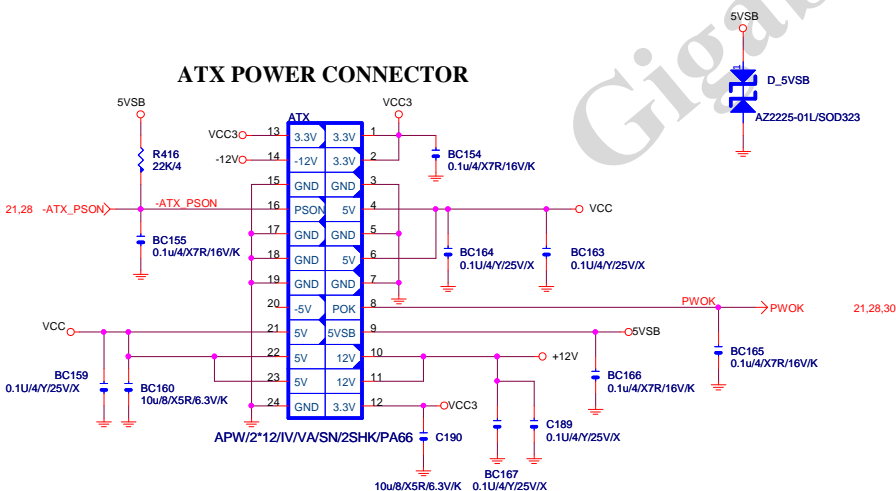
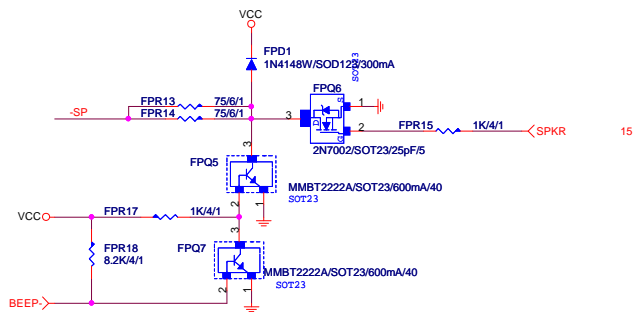
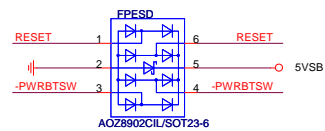
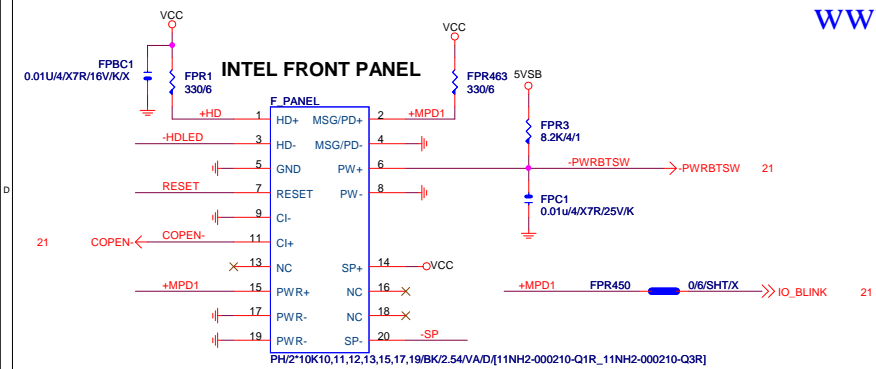


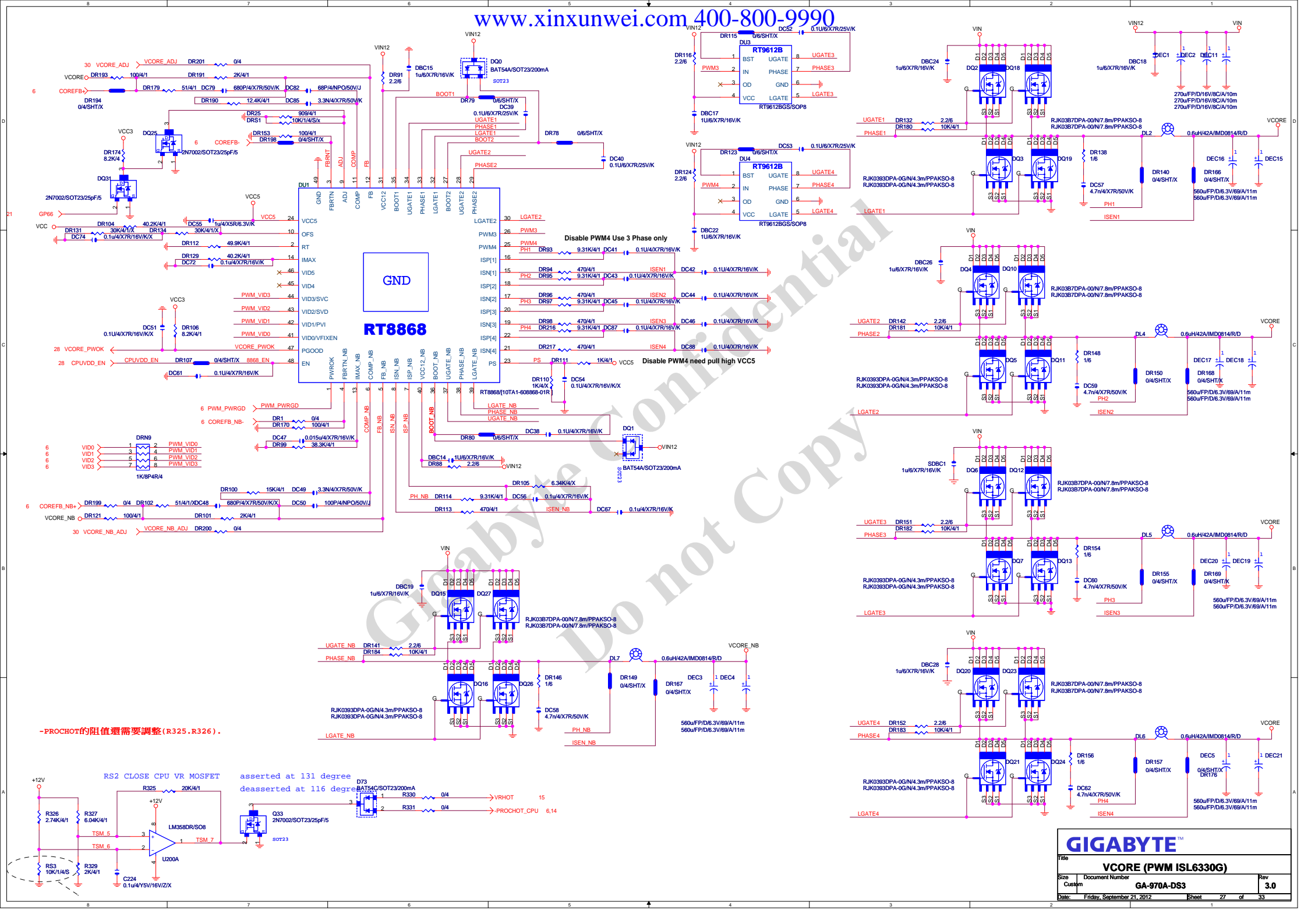


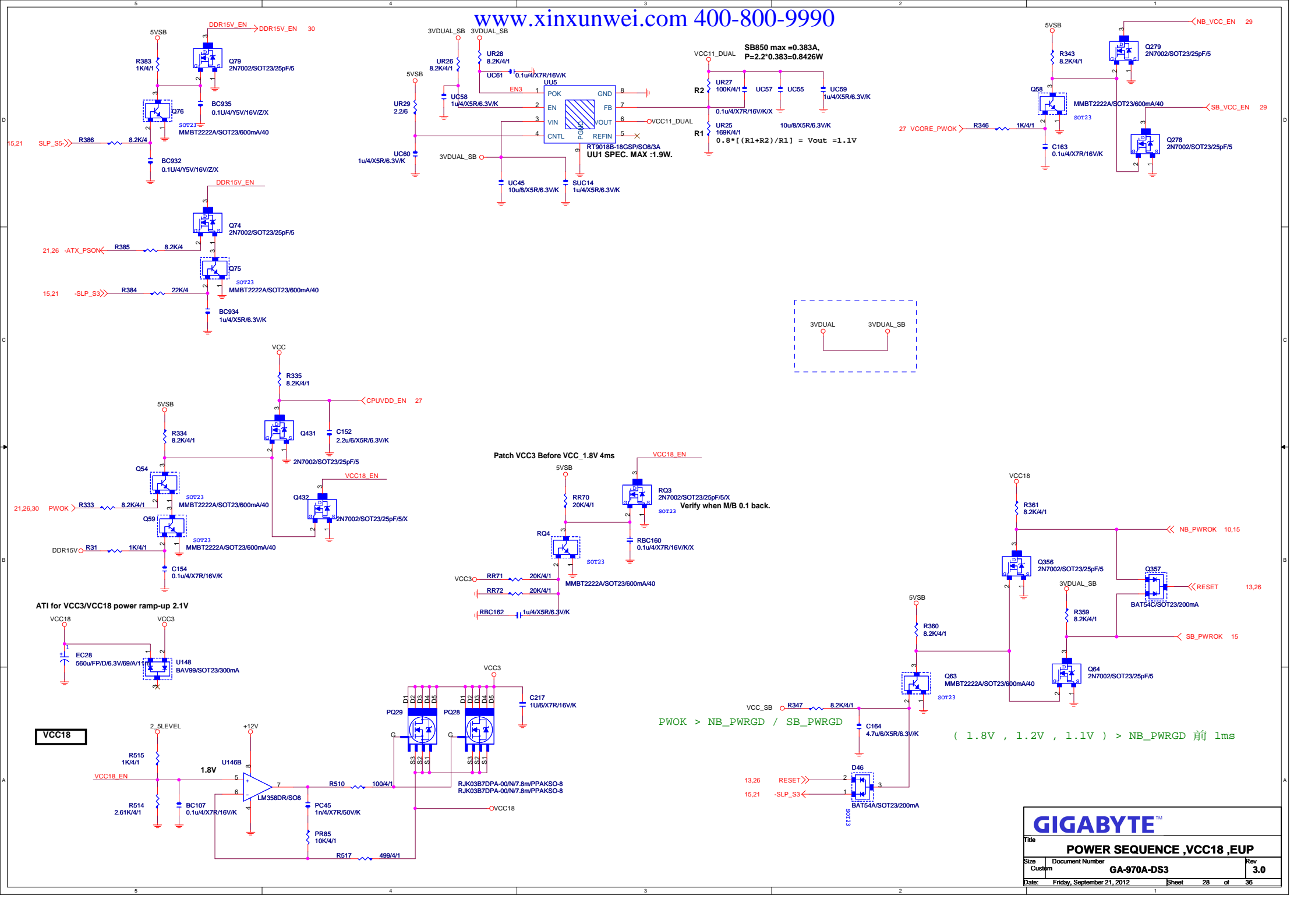
Hardware Monitor circuits



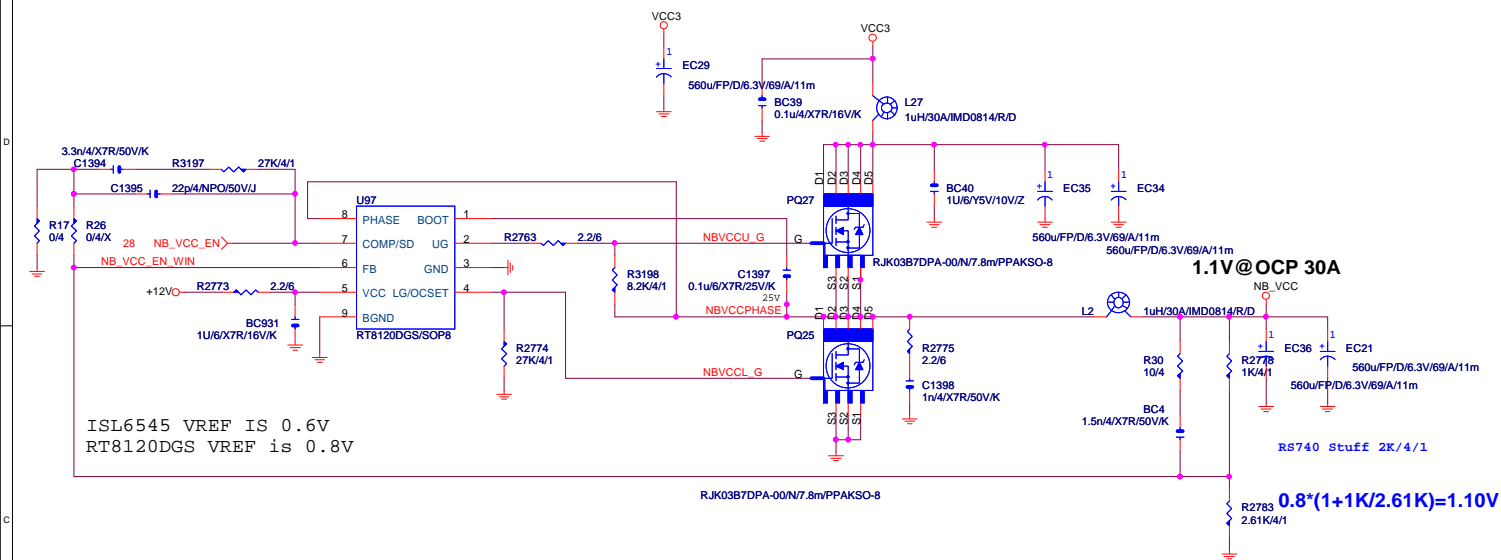
GIGABYTE
Title: FAN/HWMO KB/MS
Size: Custom Document Number: GA-970A-DS3 Rev: 3.0
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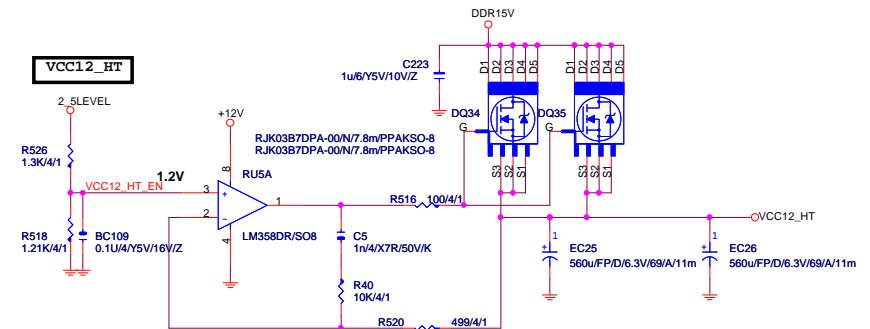




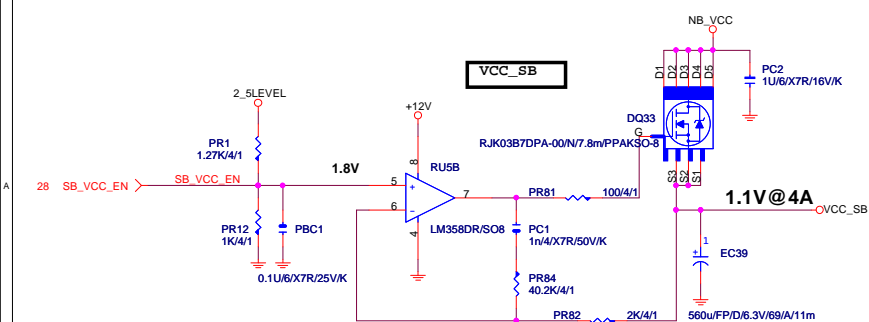
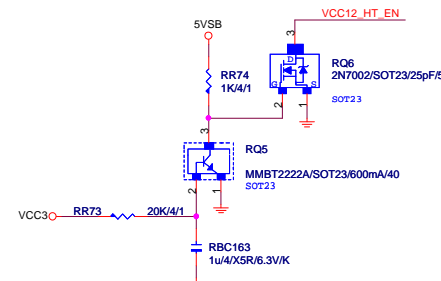
VCC_NB



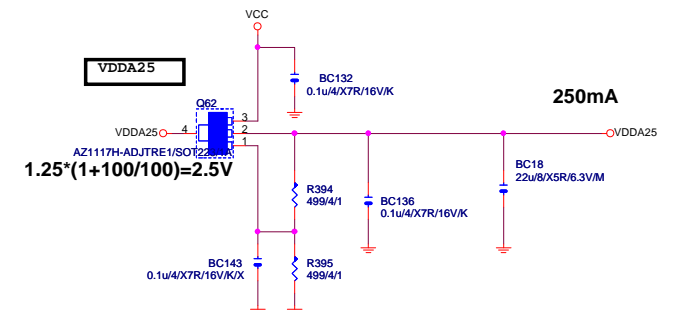
VCC12_HT



VCC_SB

Patch AMD Validation
VDDA25 & VCC12_HT
power sequence

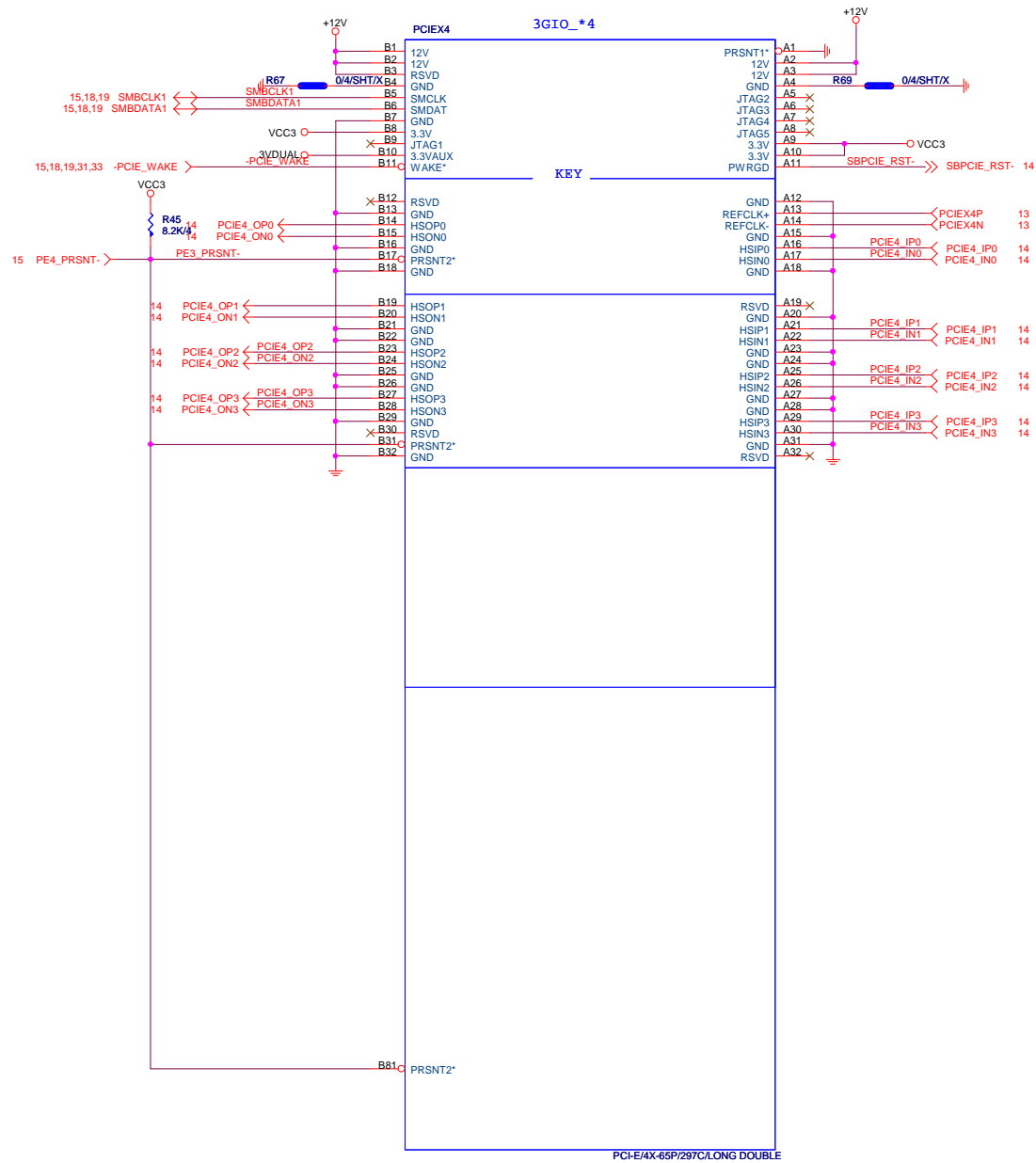
VDDA25



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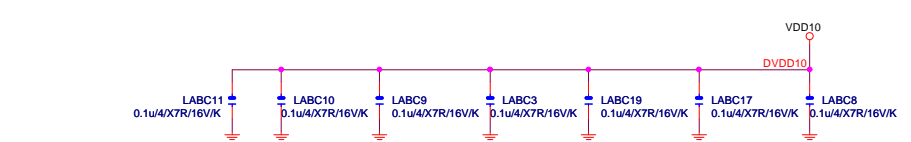
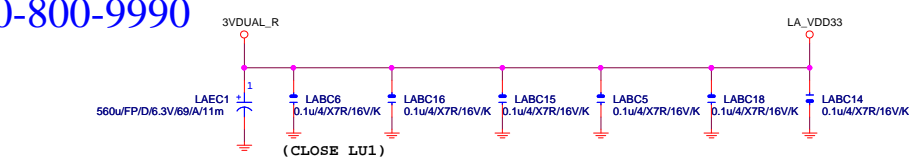
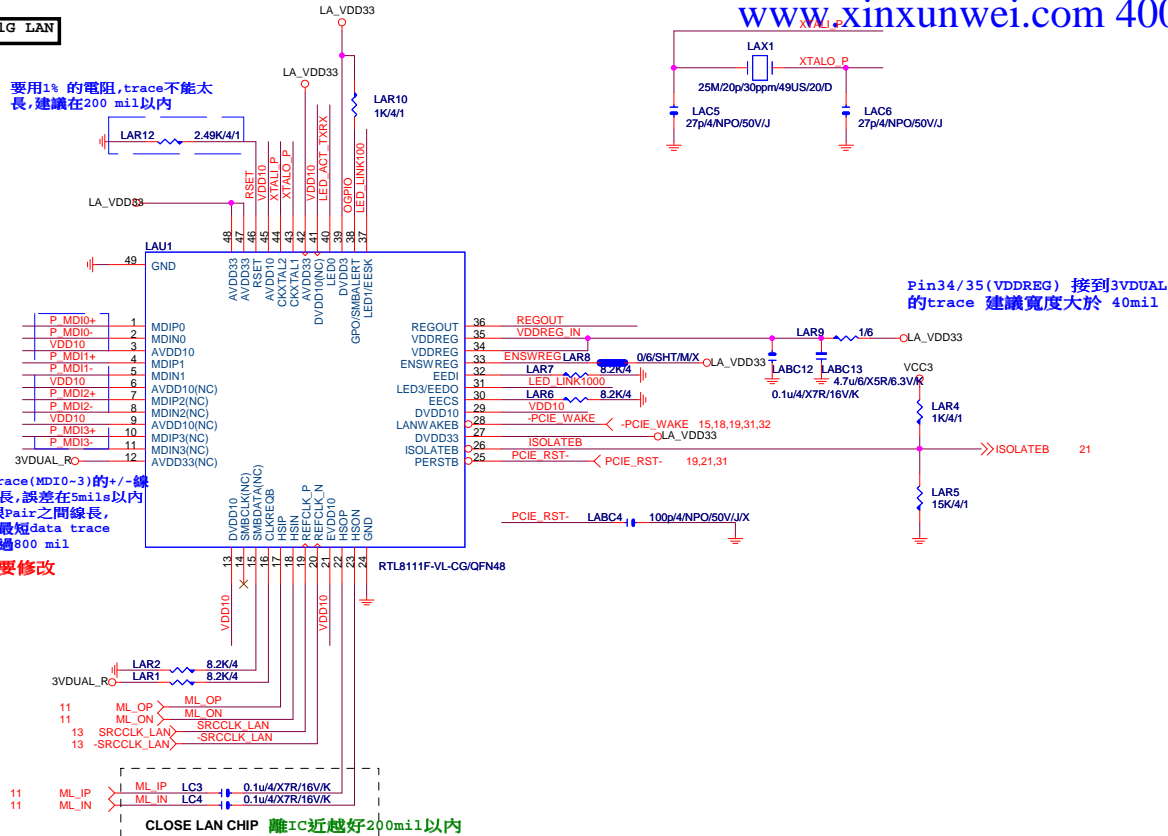


Close to USB30_LAN
90歐姆:[20/6/5.5/6/20]

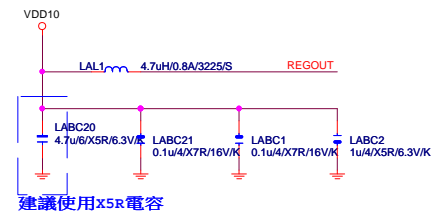
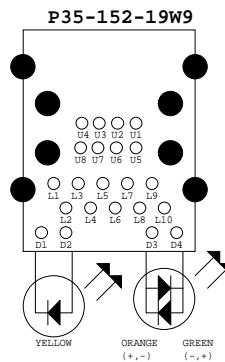


PCIE-1G LAN

要用1% 的電阻,trace不能太長,建議在200 mil以內



USB_LAN CONNECTOR

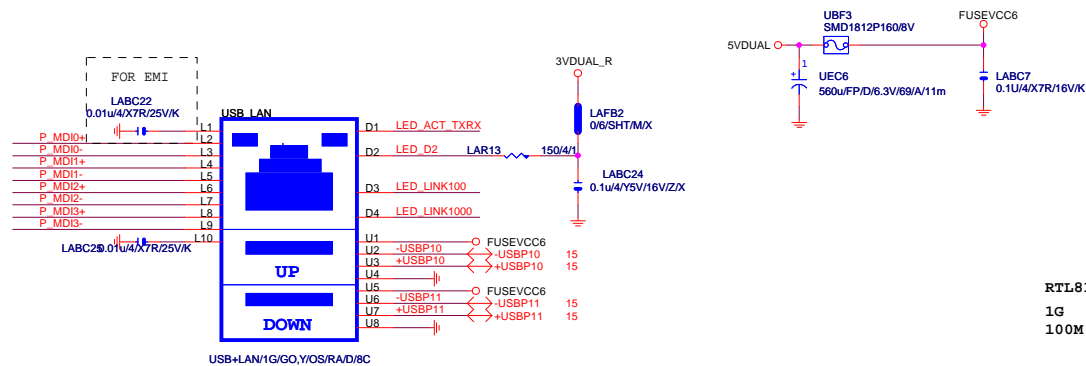
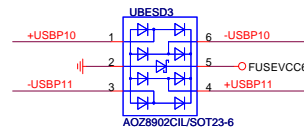


USB_LAN

RTL8101E:LR38/LC5/LR43/LC6-->0

RTL8111C:LC6-->0

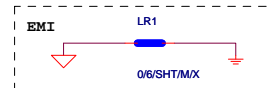
RTL8102E:LC5/LC6-->0



```
RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
```

1G :USB+LAN/1G/GO,Y/OS/RA/D/1

100M:USB+LAN/100/GO,Y/OS/RA/D/1



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